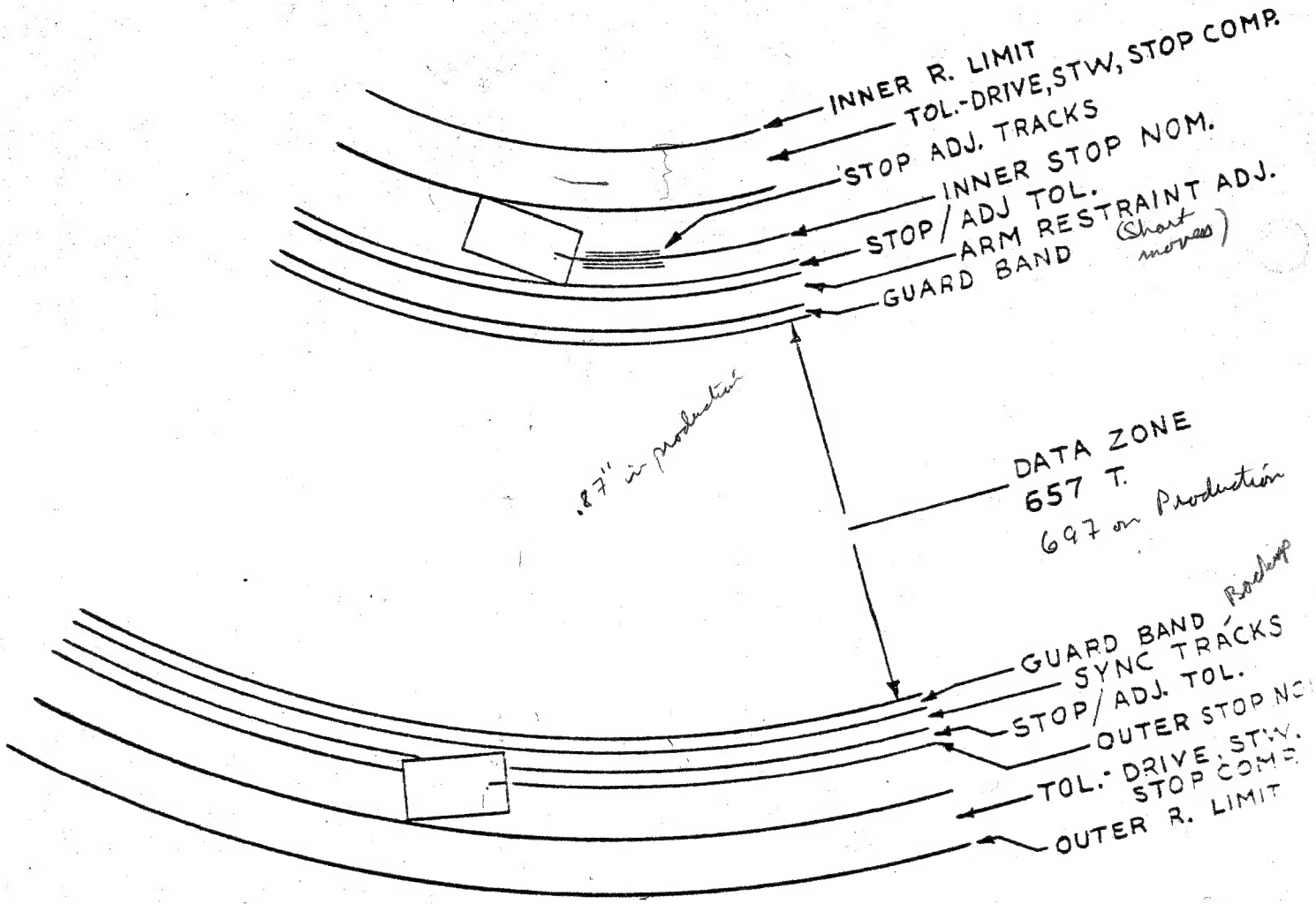
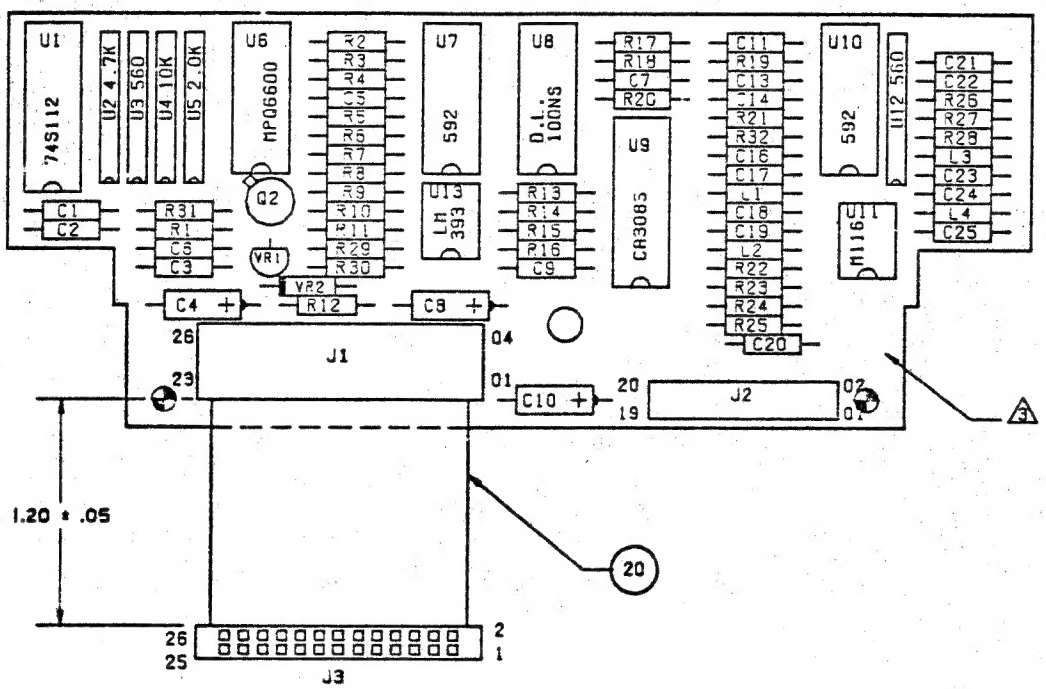
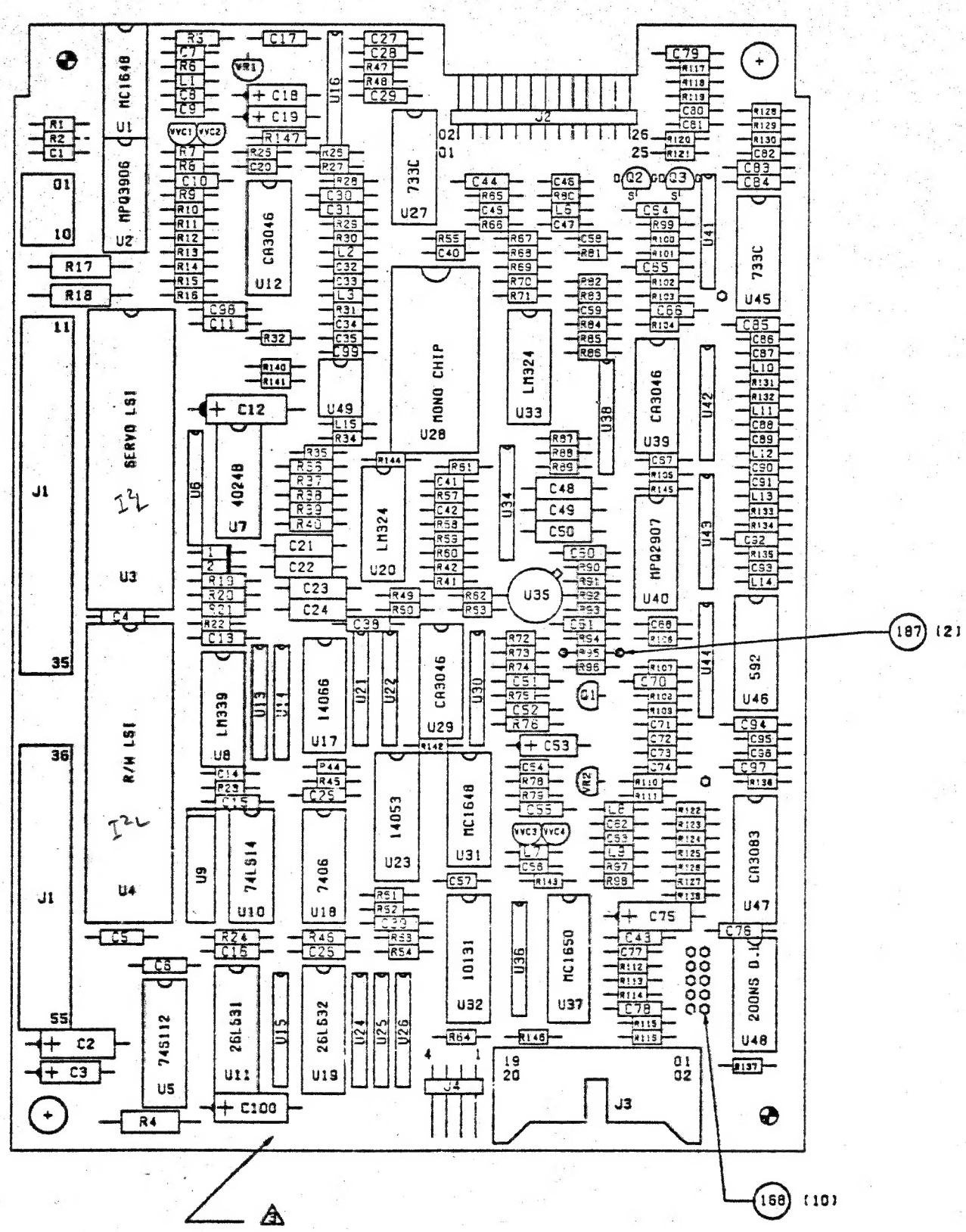
TRACK ARCHITECTURE

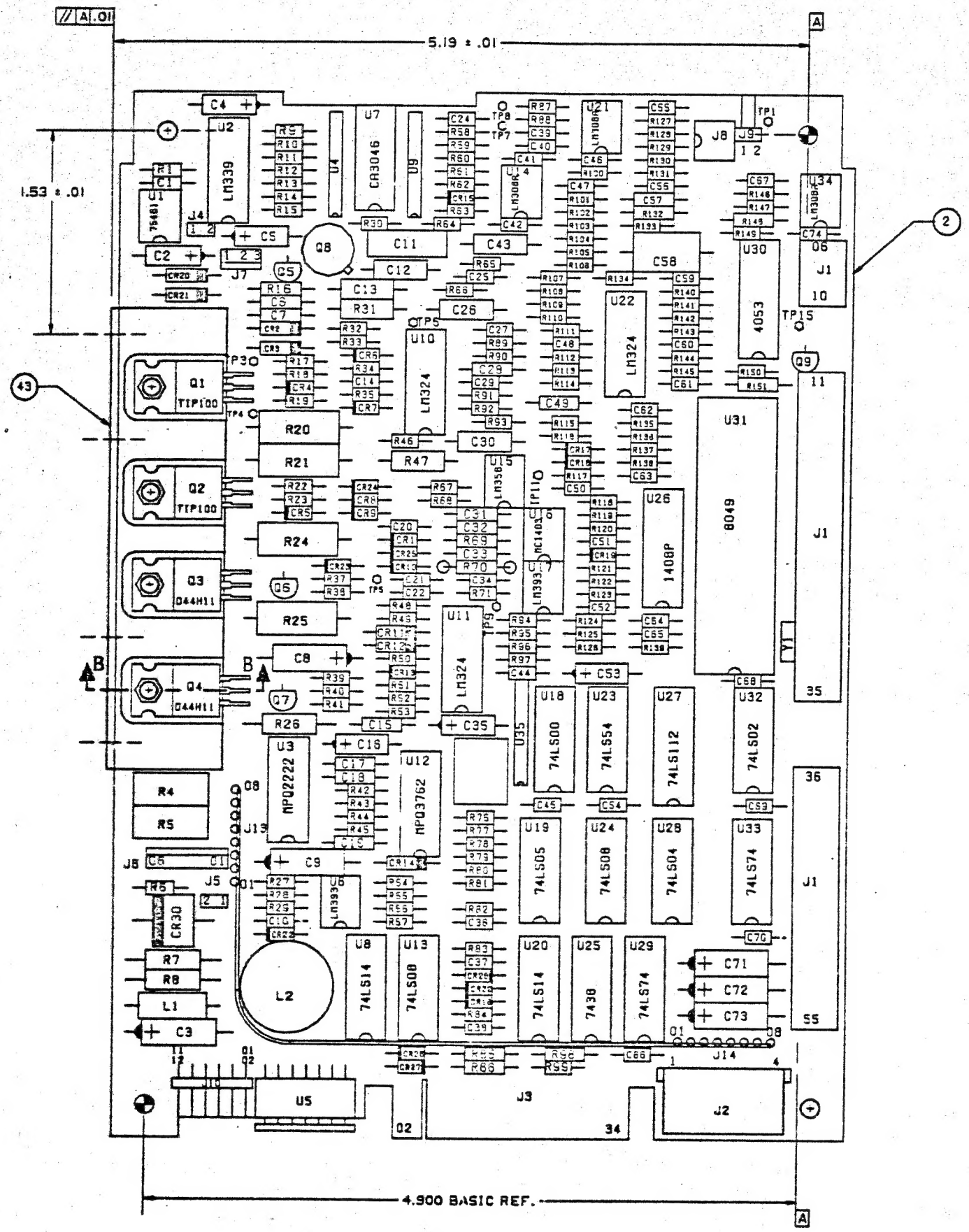




WREN PREAMP PWA



WREN -3 DATA PWA



WREN-3 SERVO PWA

BLOCK DIAGRAM

READ/WRITE SUBSYSTEM

- 5 DATA HEADS
- 5 CHANNEL LSI R/W PREAMP
- MFM RECORDING ON DISKS
- PULSE SLIMMING
- MFM/NRZ CONVERSION IN LSI (-3)
- READ PLO (-3)
- MFM INTERFACE (-5)

SERVO SUBSYSTEM

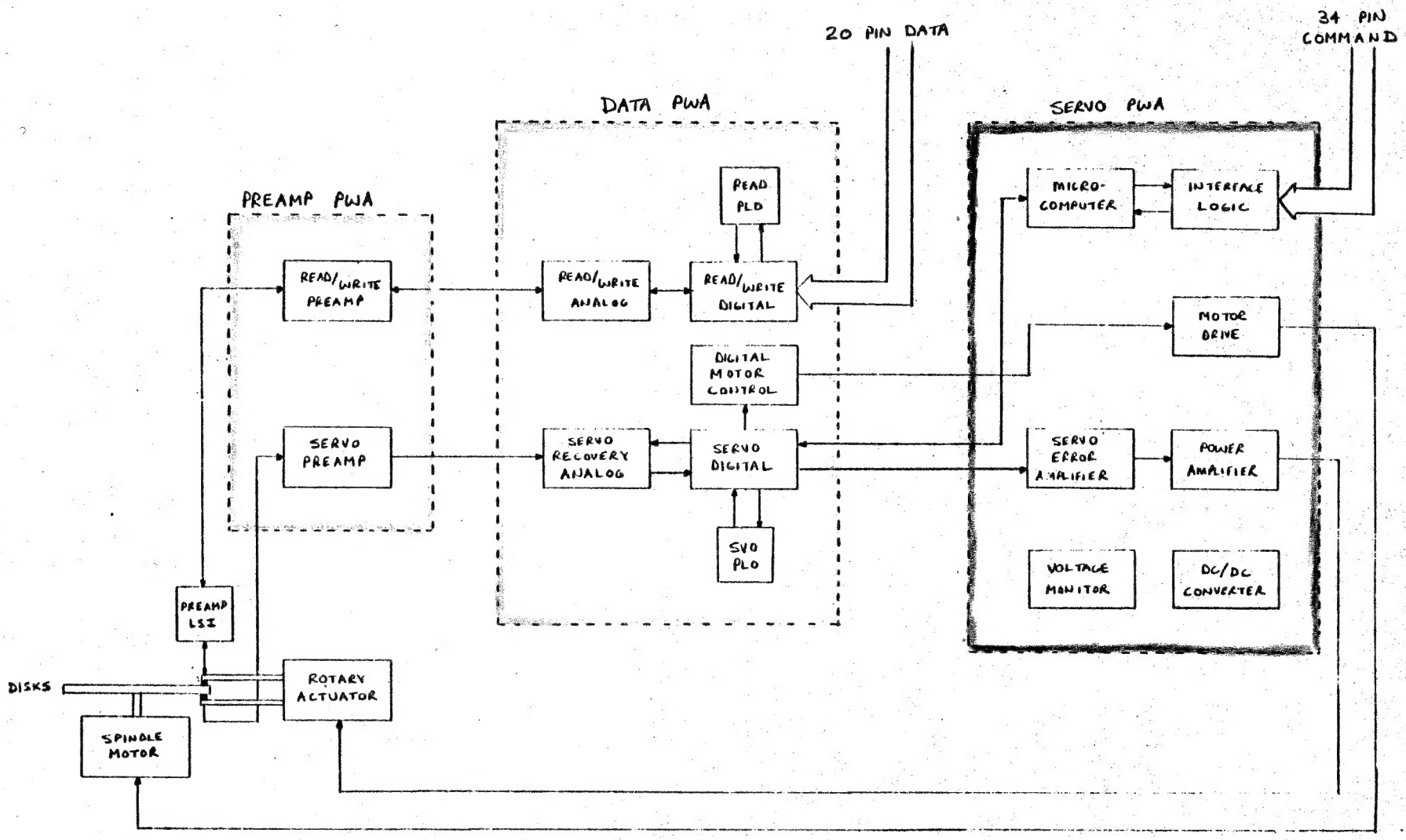
- CLOSED LOOP SERVO SYSTEM
- DEDICATED SERVO SURFACE - READ ONLY
- 8049 MICROPROCESSOR CONTROLS OPERATION
- DIGITAL LOGIC IN LSI
- ANALOG RECOVERY CIRCUITRY IN ANALOG LSI
- TWO MODES OF OPERATION
  - POSITION - ON TRACK
  - VELOCITY - SEEKING

SPINDLE MOTOR CONTROL

- CRYSTAL CONTROLLED SPEED
- DIGITAL SPEED CONTROL LOGIC IN LSI
- TWO PHASE SPINDLE MOTOR DRIVE
- CURRENT LIMITING/LOCKED ROTOR PROTECTION

OTHER ELECTRONICS

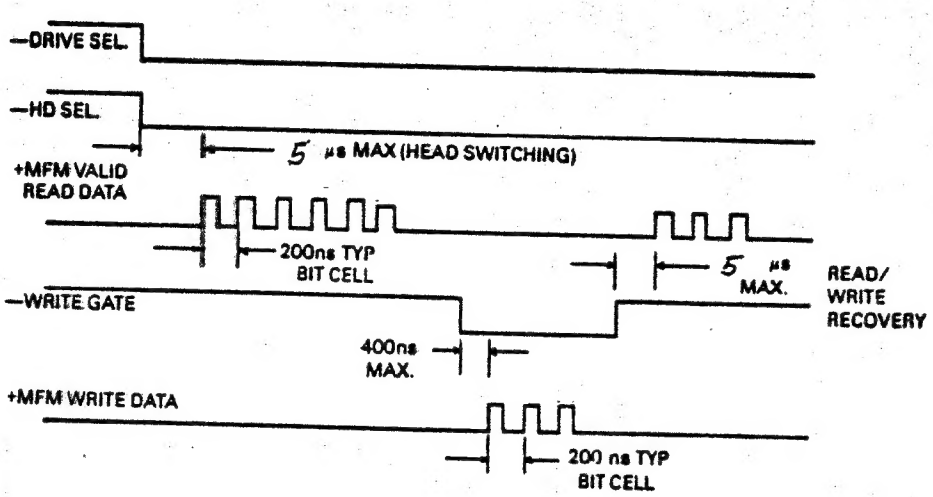
- DC/DC CONVERTER
- VOLTAGE MONITOR
- PICK AND HOLD CIRCUITS



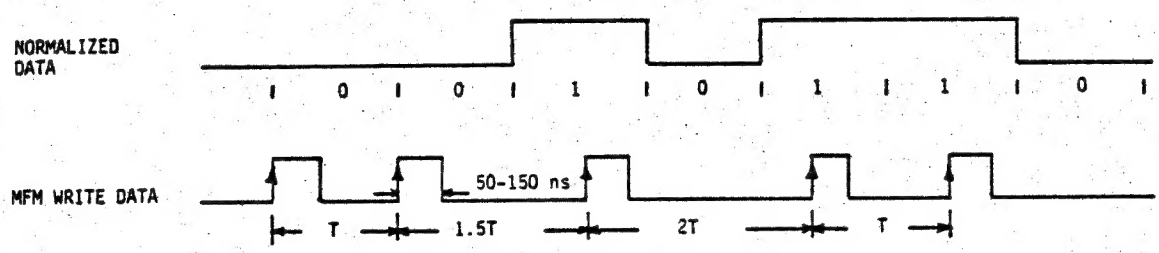
WREN -3

GENERAL BLOCK DIAGRAM

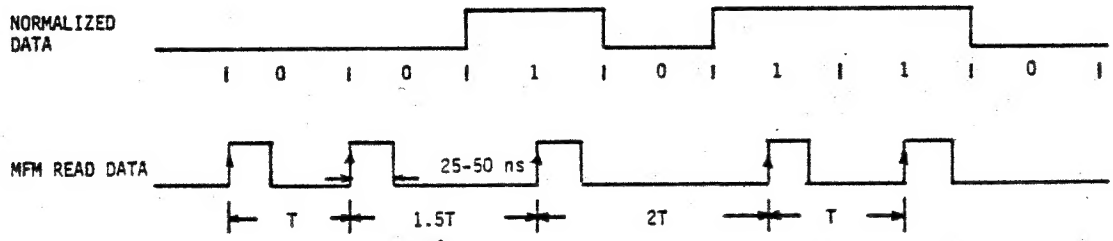
READ/WRITE DATA TIMINGS



6.2.1 -contd.



- T = 200 ns TYPICAL FOR 5.0 MHz MFM DATA RATE.
- LEADING EDGE OF WRITE DATA INITIATES WRITE TO MEDIA.
- RECOMMEND 12 ns EARLY OR 12 ns LATE WRITE PRECOMPENSATION FOR REQUIRED BIT PATTERNS.
- WRITE DATA MUST OCCUR WITHIN 400 ns FROM LEADING EDGE OF WRITE ENABLE.
- T MUST EQUAL 200 ns ± 0.25% (NOT INCLUDING WRITE COMPENSATION) AND SHOULD BE A CRYSTAL CONTROLLED WRITE FREQUENCY BY THE CONTROLLER.

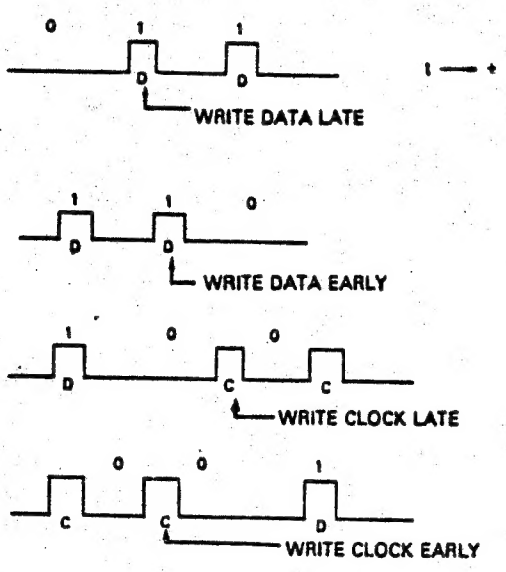


- T = 200 ns ± 1.5% FOR A 5.0 ± 0% MHz MFM WRITE DATA RATE. (LONG TERM AVERAGE)
- LEADING EDGE OF READ DATA IS CONTROLLED EDGE.
- READ DATA IS NOT VALID UNTIL 5 µs FROM TRAILING EDGE OF WRITE ENABLE OR UNTIL 5 µs AFTER A HEAD CHANGE.

FF144a

FIGURE 11. MFM DATA TIMING

WRITE PRECOMPENSATION PATTERNS



Writing should occur out of a shift register which is used to observe the pattern. "On time" represents a nominal delay. Early and late represent less and more delay respectively.

"A1" ADDRESS MARK BYTE

Bit Position

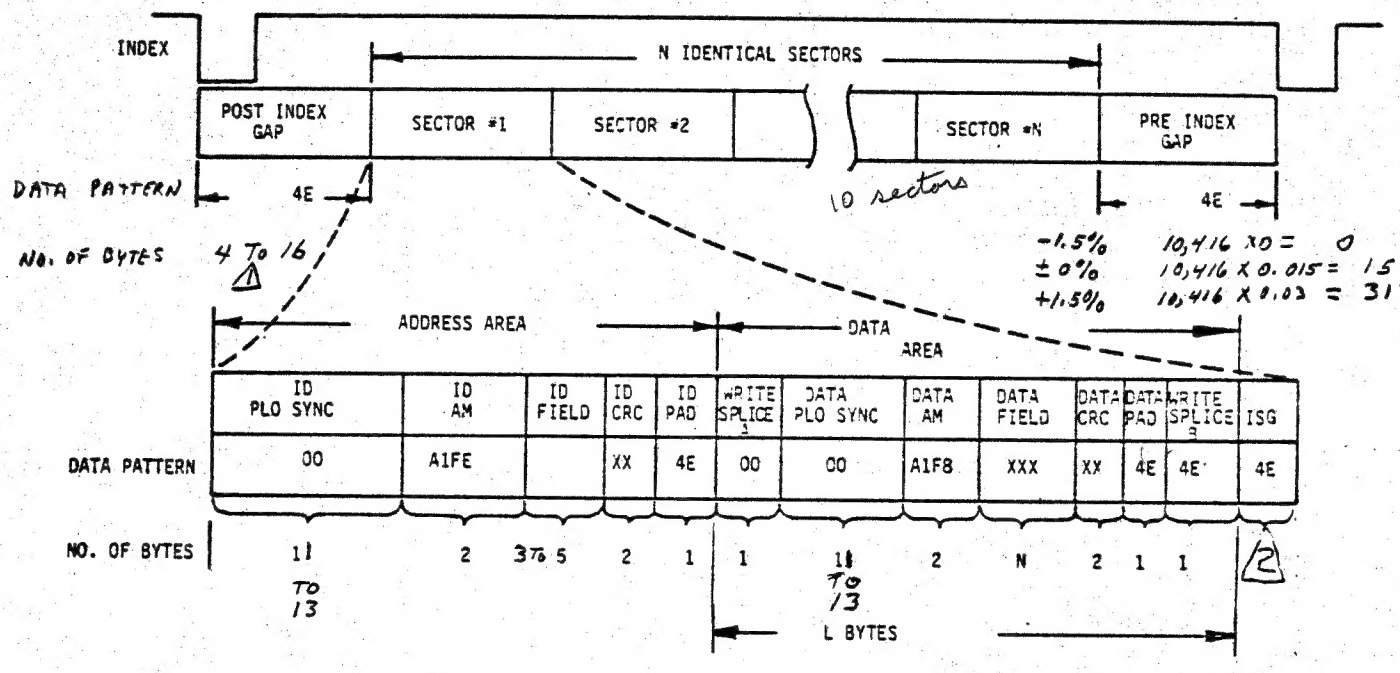
	0		1		2		3		4		5		6		7	
	C	D	C	D	C	D	C	D	C	D	C	D	C	D	C	D
"A1" Data Bits		1		0		1		0		0		0		0		1
"A1" Clock Bits		0		0		0		0		1		0		1		0

Encoded pattern with dropped clock

Normal encoded pattern without dropped clock

D D C C C D

C = clock bit
D = data bit



⚠1 4 FOR HEAD SWITCH AND WRITE TO READ RECOVERY

12 FOR ST412 COMPATIBILITY

16 FOR ST 506/ST412 COMPATIBILITY

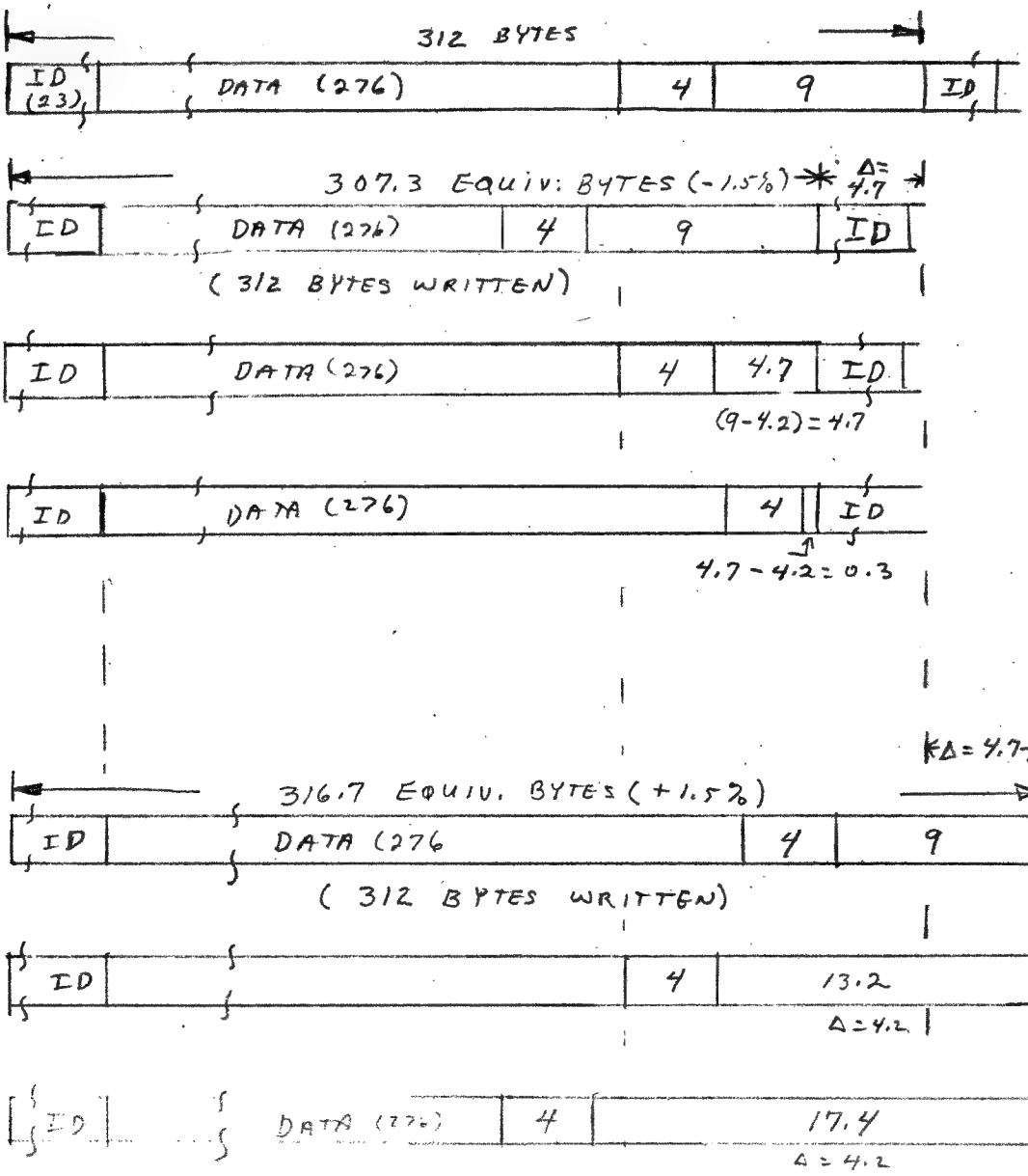
⚠2
- $(4 + 0.03L) \pm (0.03L)$ BYTES {i.e. $-(4)$ TO $(4 + 0.06L)$}
- TOTAL TOLERANCE AFTER FORMAT IS ±1.5%
- DURING FORMAT WRITE $(4 + 0.03L)$ BYTES
- 4 BYTES IS FOR WRITE TO READ RECOVERY, AND INTERFACE WRITE DATA TO MEDIA WRITE DELAY
- FOR 256 BYTE DATA FIELD ISG IS:

−3%	≈ 4 BYTES	VARANCE IF WRITE TOLERANCE AT FORMAT WAS −1.5%
−1.5%	≈ 9 BYTES	
±0%	≈ 13 BYTES	VARANCE IF WRITE TOLERANCE AT FORMAT WAS 0.0%
+1.5%	≈ 17 BYTES	
+3.0%	≈ 21 BYTES	VARANCE IF WRITE TOLERANCE AT FORMAT WAS +1.5%

NOTES:

1. ALL PATTERNS SHOWN IN THE VARIOUS FIELDS ARE IN HEX
2. ALL "X's" REPRESENT VARIABLE FIELDS
3. FORMAT ASSUMES ±1.5% TOTAL WRITE TOLERANCES
   i.e. ±1% DRIVE SPINDLE SPEED
   ±0.25% DRIVE ELECTRONICS
   ±0.25% CONTROLLER WRITE FREQUENCY/ELECTRONICS
4. ID FIELD CONTAINS FLAG(S), CYLINDER, SECTOR ADDRESS

MINIMUM RECOMMENDED TRACK/SECTOR FORMAT



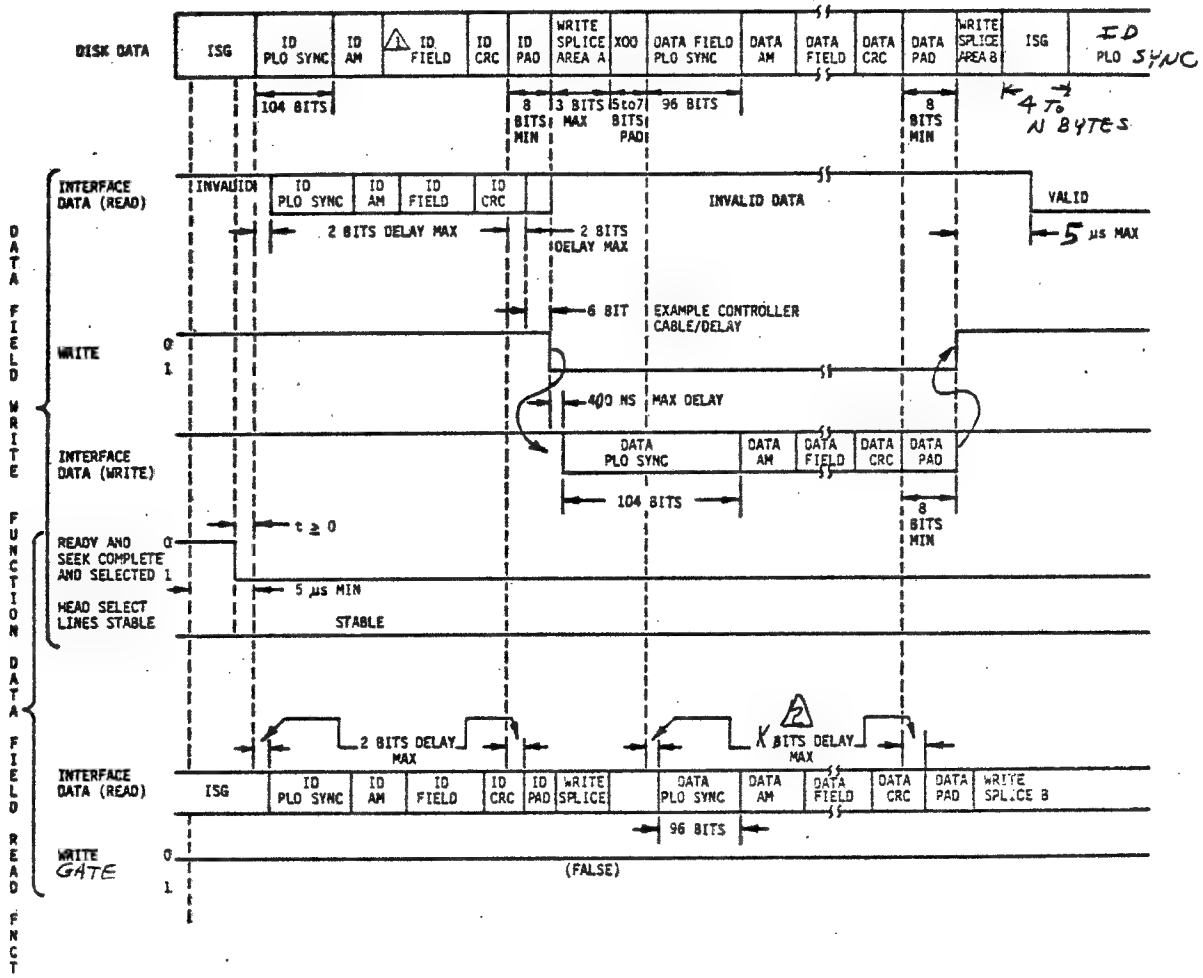
ID = 23 BYTES

DATA = 276 BYTES

FORMAT ISG = $\frac{13 \text{ BYTES}}{312 \text{ BYTES}}$ = 4 + (.03)(276) = 4 + 8.3

ISG VARIATIONS

7.3.1 -contd.



1 THE ID FIELD INCLUDES THE TRACK, HEAD, AND SECTOR LOCATION.

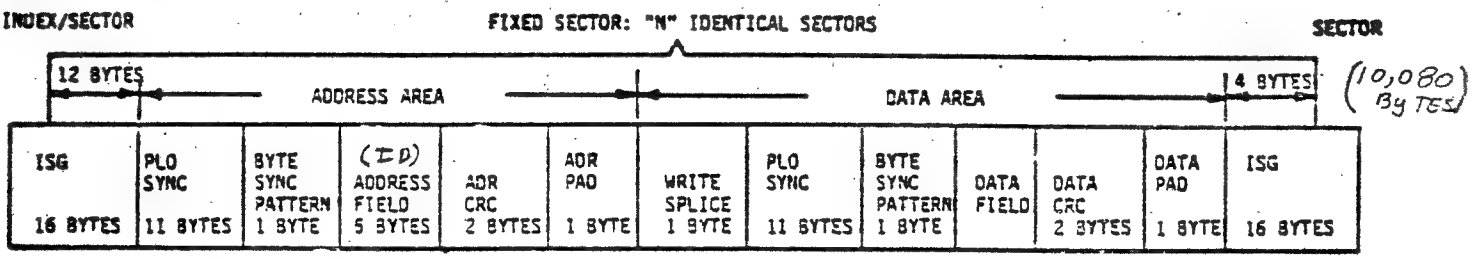
FF138

2 - K = 2 BITS(MAX) From where DATA IS STORED ON THE MEDIA

NOTE: AFER A DATA FIELD WRITE UPDATE, PER THIS FIGURE) THE DATA FIELD MAY BE SHIFTED UP TO 4 BIT LOCATIONS TO THE RIGHT ON THE MEDIA (i.e. 2 BITS DUE TO 400 nsec WRITE GATE TO WRITE DATA DELAY plus 2 BITS DUE TO DRIVES INTERNAL WRITE PROPAGATION DELAY)

FIGURE 14. TYPICAL READ/WRITE TIMING

9415-3 WREN FORMAT



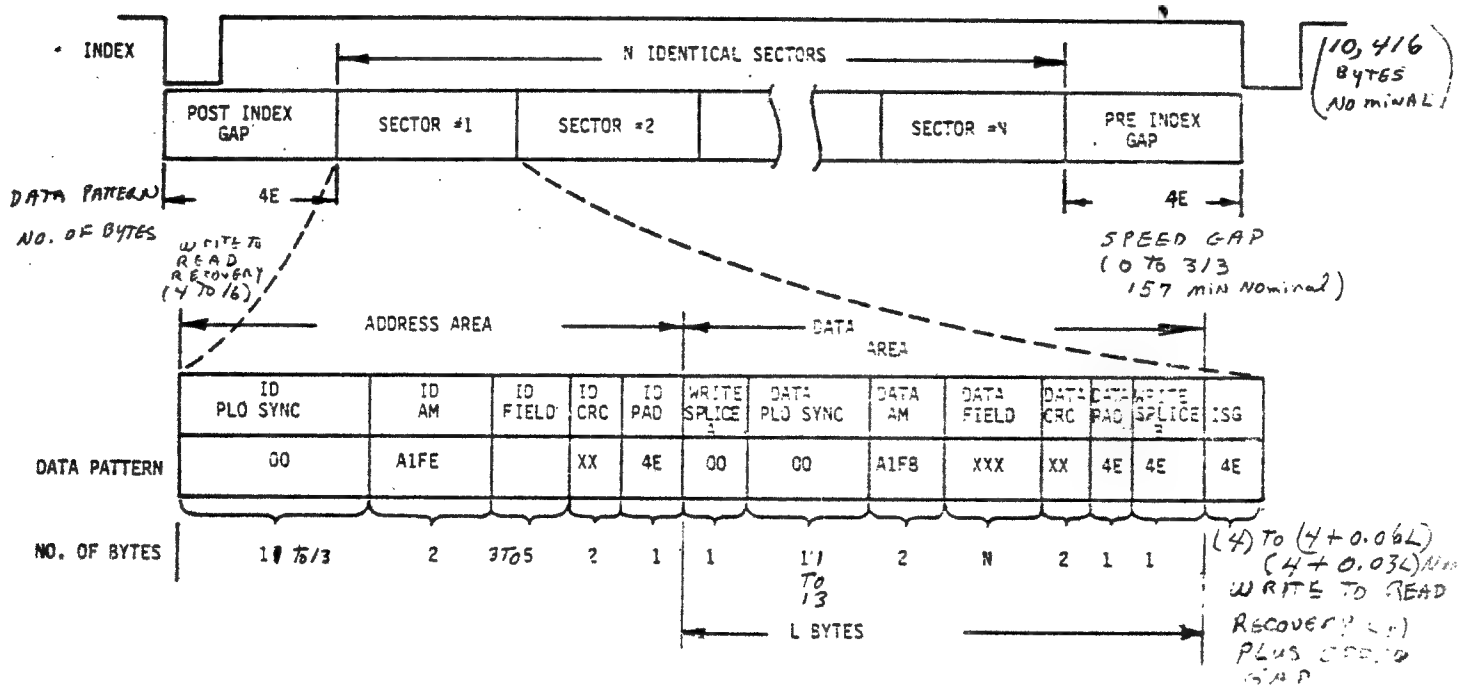
NOTES: 1. SECTOR PULSES GENERATED BY CONTROLLER AND DERIVED FROM DRIVE SUPPLIED INDEX AND BYTE CLOCK. ID FIELD AFTER SECTOR/INDEX.

2. • HEAD SWITCH TO READ/WRITE = 15 μs ⇒ 9.1 BYTES
   • WRITE TO READ RECOVERY = 10 μs ⇒ 6.1(7) BYTES

3. NO SPEED GAPS REQUIRED

4. ALLOWS 32 SECTORS of 256 DATA BYTES PER SECTOR
   $\frac{10,080}{32}$ = 315 BYTES/SECTOR Available (308 BYTES/SECTOR SHOWN above)

9415-5 WREN FORMAT



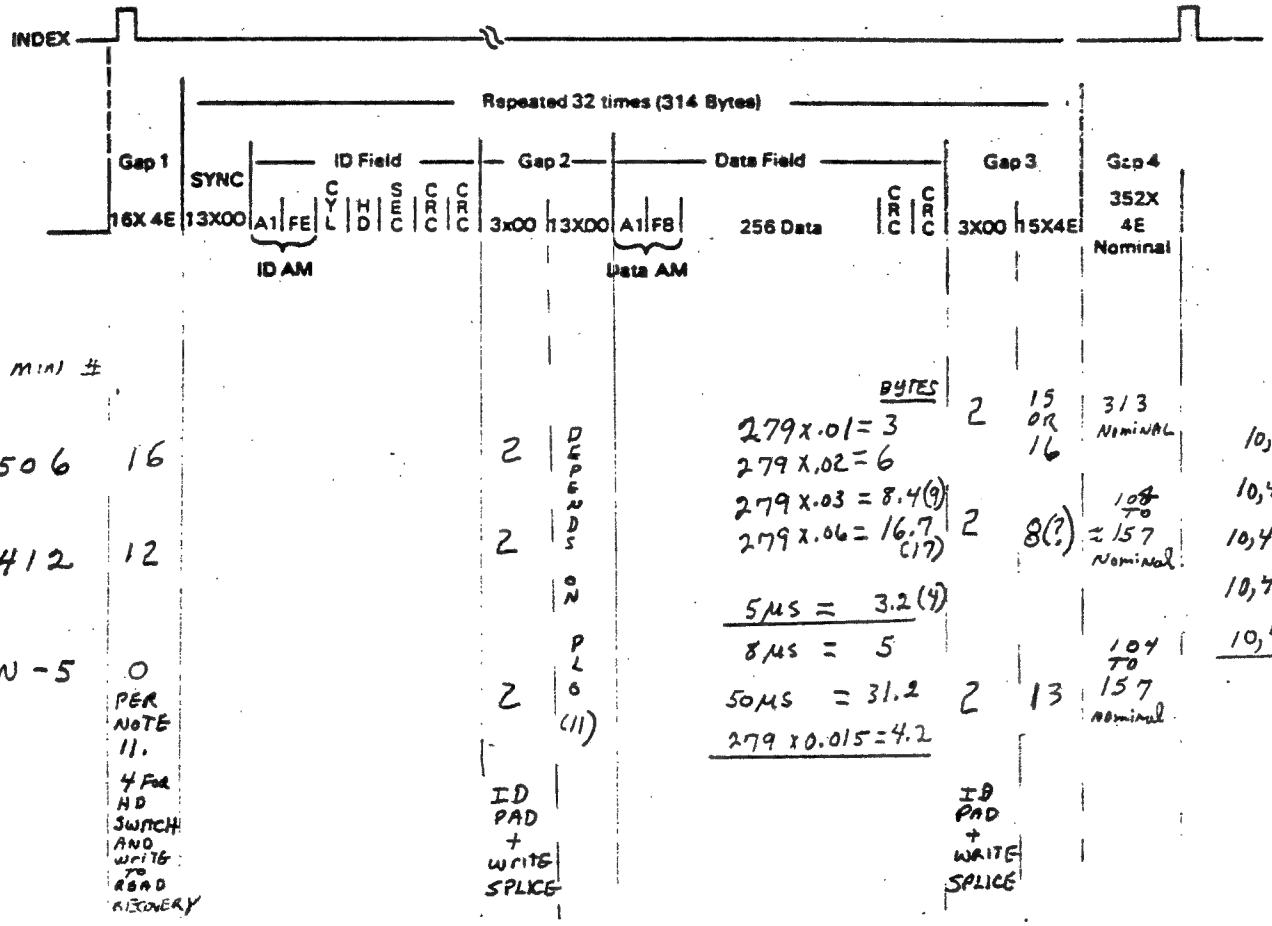
NOTES: 1. ID FIELD AFTER ID AM which contains ILLEGAL MISSING CLOCK.

2. • HEAD switch To READ/WRITE = 5 μs ⇒ 3.2(4) BYTES
   • WRITE To READ RECOVERY = 5 μs ⇒ 3.2(4) BYTES

3. SPEED GAPS REQUIRED.

4. ALLOWS 32 SECTORS OF 256 BYTES PER SECTOR
   MAX BYTES per sector Available = (10,416 − 16 − 313) ÷ 32 = 315.
   (306 To 312 BYTES/SECTOR SHOWN above)

TRACK FORMAT AS SHIPPED (ST 506 AND ST 412)



NOTES:

1. Nominal Track Capacity = 10416 Bytes
2. Total Data Bytes/Track = 256 x 32 = 8,192
3. Sector interleave factor is 4. Sequential ID Fields are sector numbered 0, 8, 16, 24, 1, 9, 17, 25, 2, 10, 18, 26....etc.
4. Data Fields contain the bit pattern 0000 as shipped
5. CRC Fire Code $=x^{16}+x^{12}+x^{5}+1$
6. Bit 7 of Head Byte ID Field equals 1 in a defective sector (Cylinder 0 is error free)
7. Bit 5 of Head Byte reserved for numbering cylinders greater than 256
8. Bit 6 of Head Byte reserved for numbering cylinders greater than 512

9. **Gap 3**

   Gap 3 following each data field allows for the spindle speed variations. This allows for the situation where a track has been formatted while the disc is running faster than nominal, then write updated with the disc running slower than normal. Without this gap, or if it is too small, the sync bytes or ID field of the next field of the next field could be over written. As shipped, the gap allows a ±3% speed variation (actual drive spec is ±1%). Minimum gap is 8 bytes for a 256 byte record size.

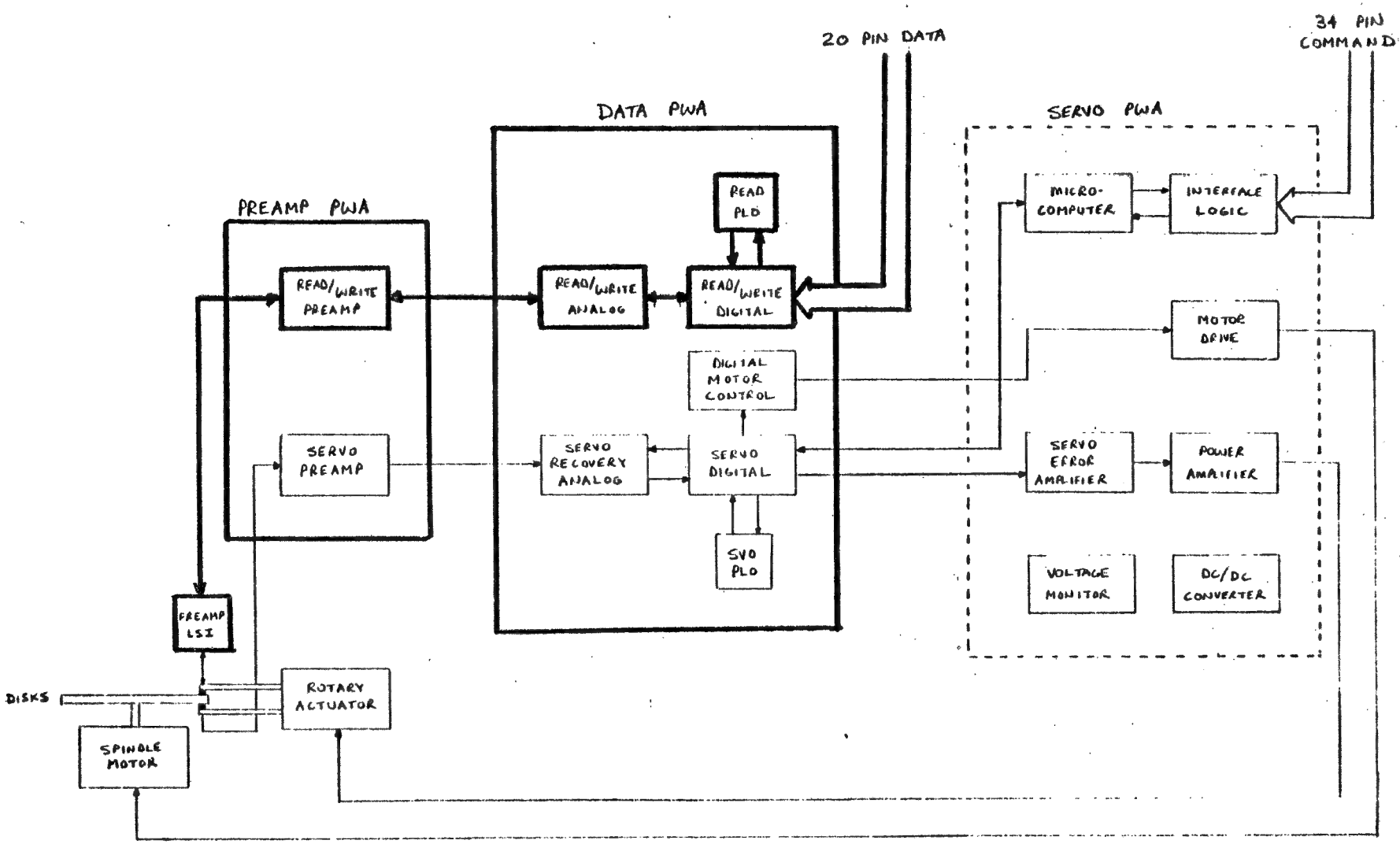
10. **Gap 4**

    Gap 4 is a speed tolerance buffer for the entire track, which is applicable in full track formatting operations to avoid overflow into the index area. The format operation which writes ID fields begins with the first encountered index and continues to the next index. The actual bytes in Gap 4 depends on the exact rotating speed during the format operation.

11. **Gap 1**

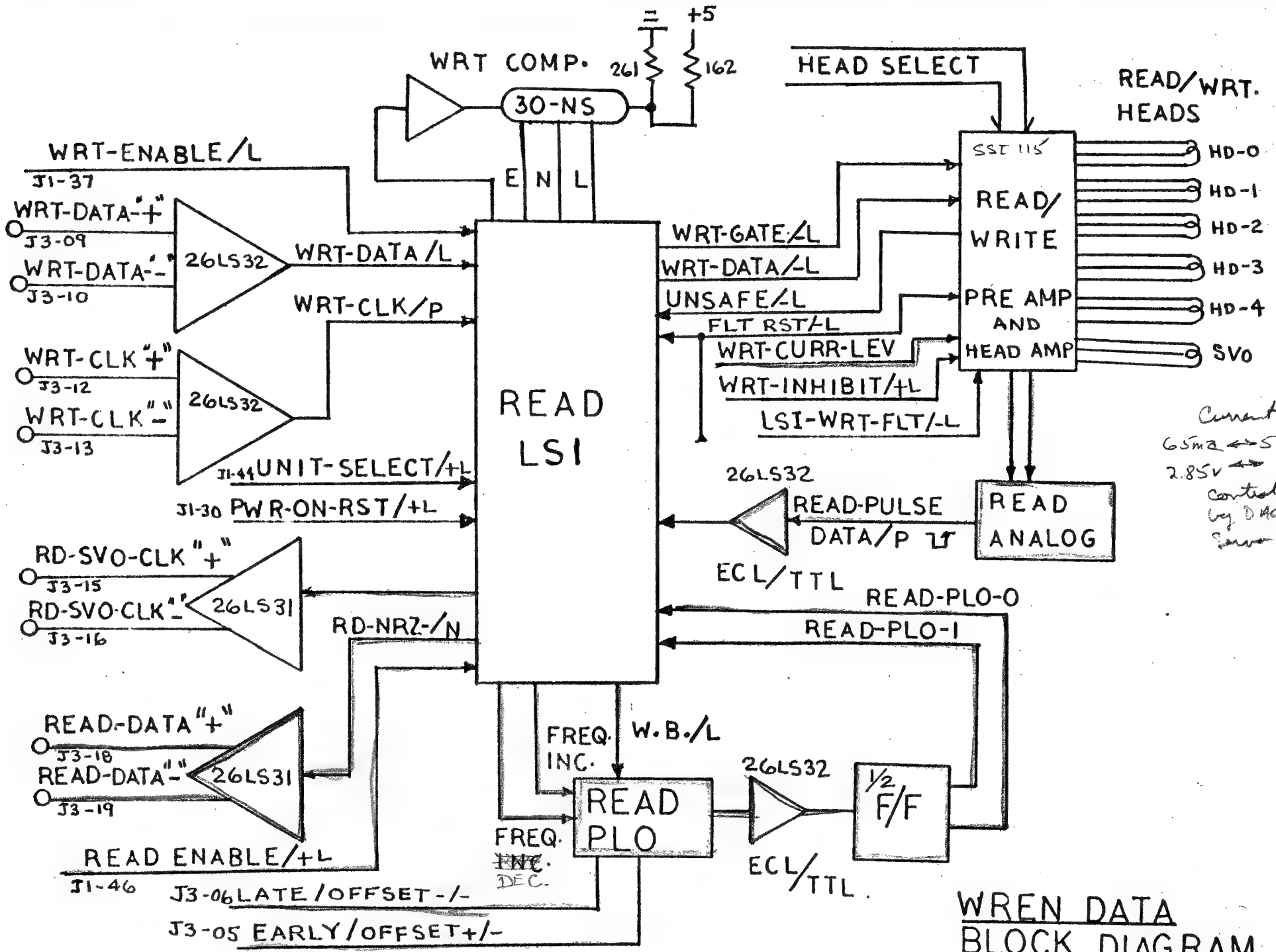
    Gap 1 is to provide for variations in index detection. As shipped, gap 1 is 16 bytes long, but must be at least 12 bytes. Gap 1 is immediately followed by a sync field preceding the first ID field.

WREN - READ/WRITE



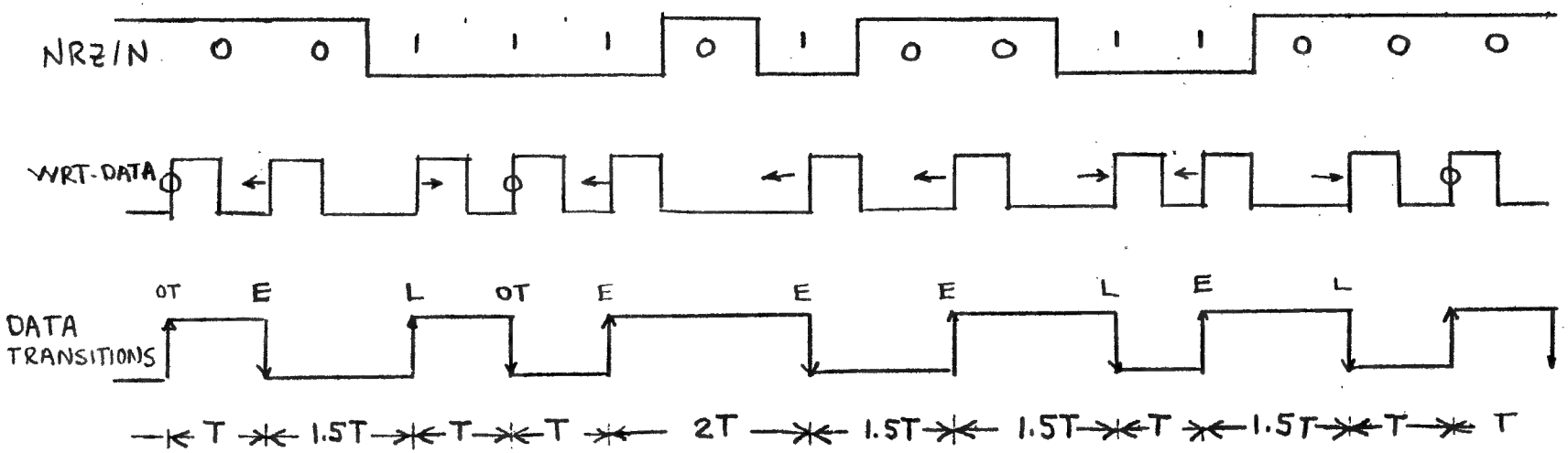
WREN -3

GENERAL BLOCK DIAGRAM



WREN DATA BLOCK DIAGRAM

EDDY MILANES 382

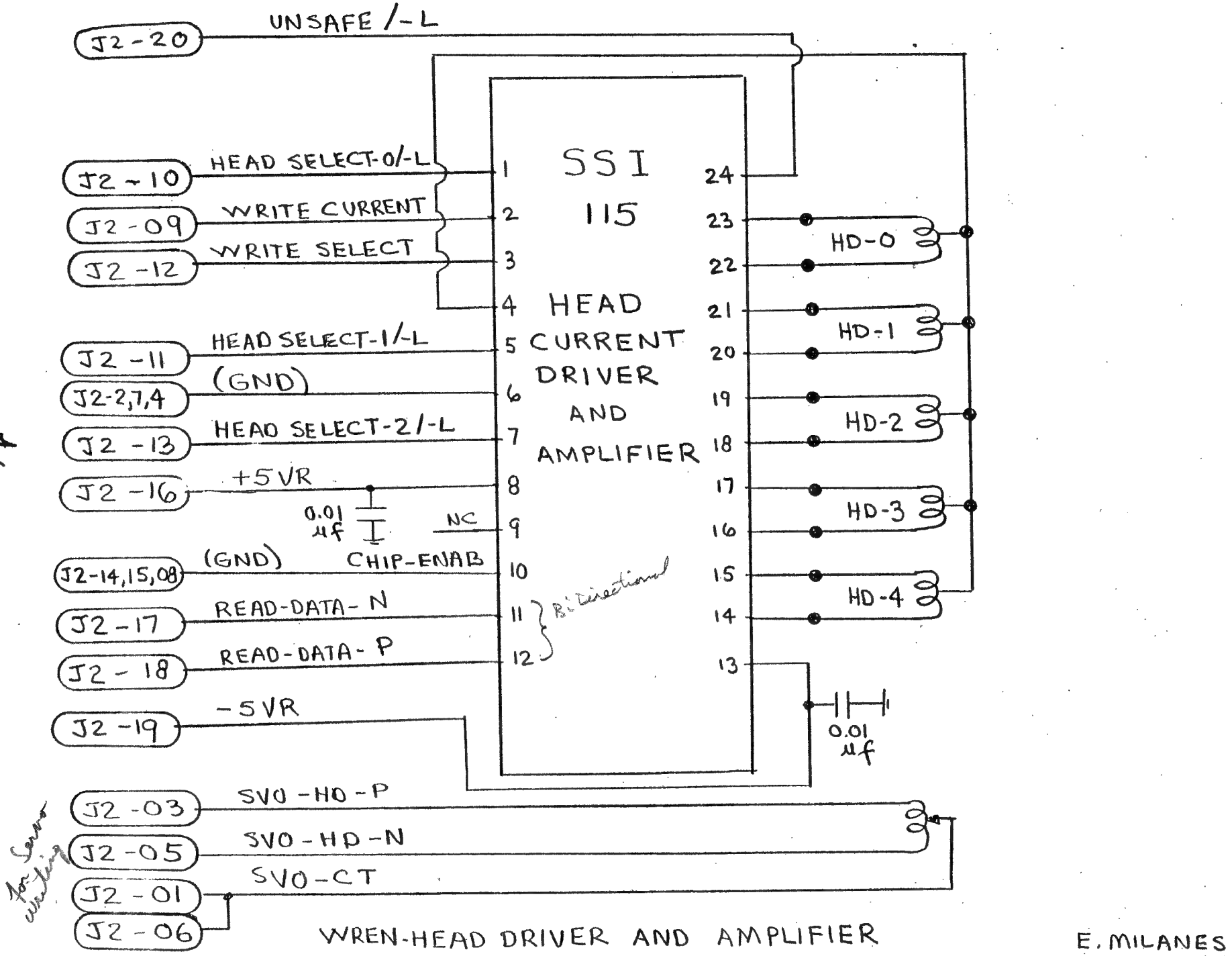


COMPENSATED MFM WAVE FORM

WREN READ/WRITE HEAD PREAMP

- FIVE CHANNEL INTEGRATED CIRCUIT - SSI115.
- MOUNTED ON ACTUATOR CLOSE TO DATA HEADS TO IMPROVE SIGNAL-TO-NOISE RATIO.
- WRITE CURRENT PATHS TO DATA HEADS ARE KEPT SHORT TO MINIMIZE WRITE-TO-SERVO CROSSTALK.
- COMMON FLEX CABLE FOR READ/WRITE AND SERVO SIGNALS.
- PREAMP HAS VERY LOW NOISE CHARACTERISTICS AND HIGH GAIN (26-52). 200-250 μv on inner tracks
- LOW LEVEL READ SIGNALS FROM THE HEADS ARE AMPLIFIED BEFORE BEING SENT OUTSIDE THE SEALED CHAMBER.

output 10-20 mv



WREN-HEAD DRIVER AND AMPLIFIER

E. MILANES

WREN READ/WRITE PREAMPLIFIER PWA

SERVO SIGNAL PATH

8 pin Dip SSI M116

- LOW NOISE (0.8-1.1 nv/$\sqrt{HZ}$), HIGH GAIN (250) PREAMPLIFIER FOR SERVO SIGNAL AMPLIFICATION.
- 3 POLE LOW PASS LINEAR FILTER FOR HIGH FREQUENCY NOISE REJECTION. Very low noise

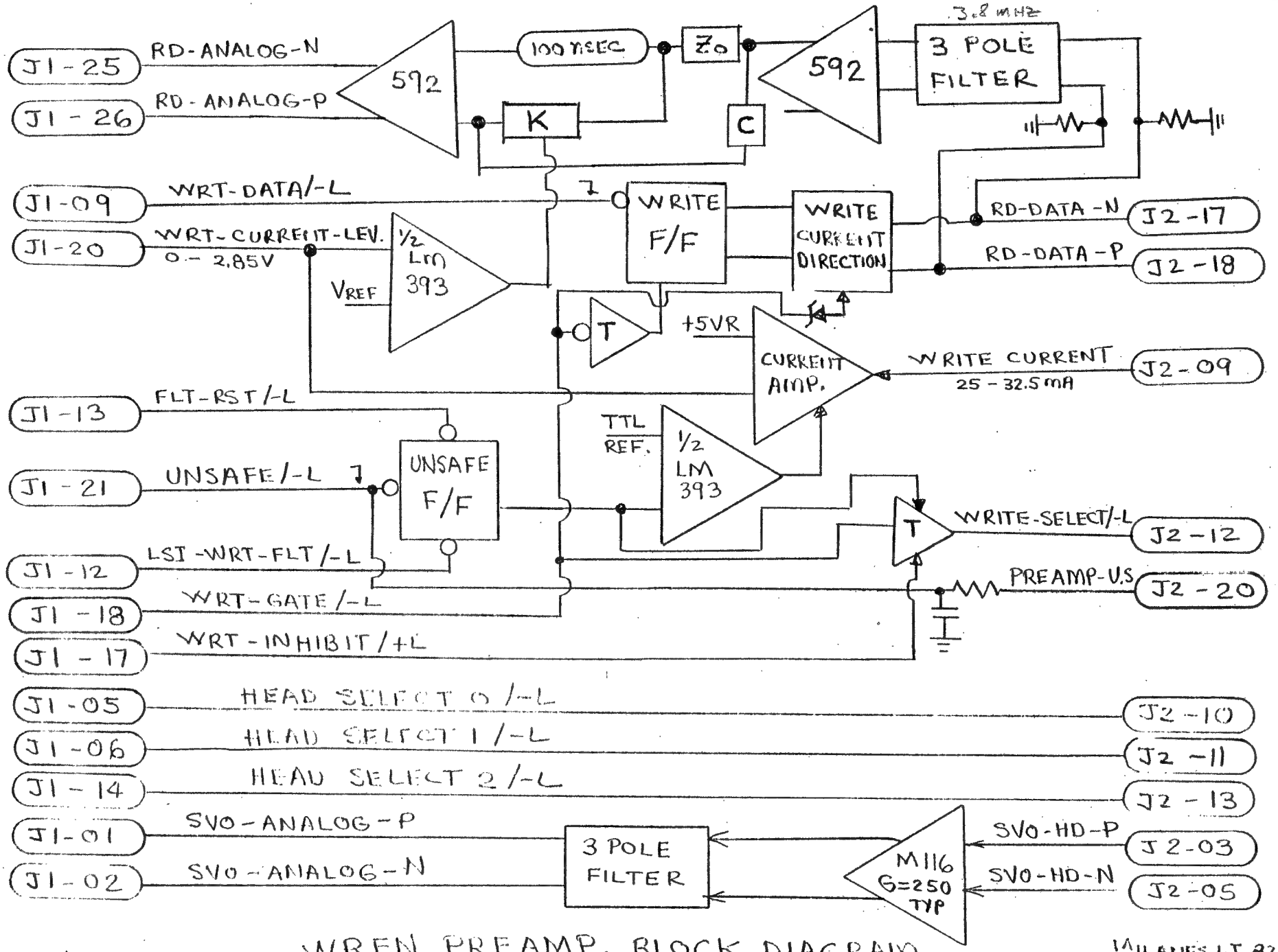
1.8 MHz for Servo

READ DATA SIGNAL PATH

- 3 POLE LOW PASS LINEAR PHASE FILTER FOR HIGH FREQUENCY NOISE REJECTION.
- TRANSVERSAL FILTER FOR PULSE SLIMMING.
  - SWITCHED GAIN PULSE SLIMMER. Uses write current DAC to change gain. Low at outer tracks
  - OPTIMIZED SIGNAL AT INNER AND OUTER CYLINDERS.
  - SIGNAL CORRECTION FACTOR C GIVES ADDITIONAL SIGNAL IMPROVEMENT.

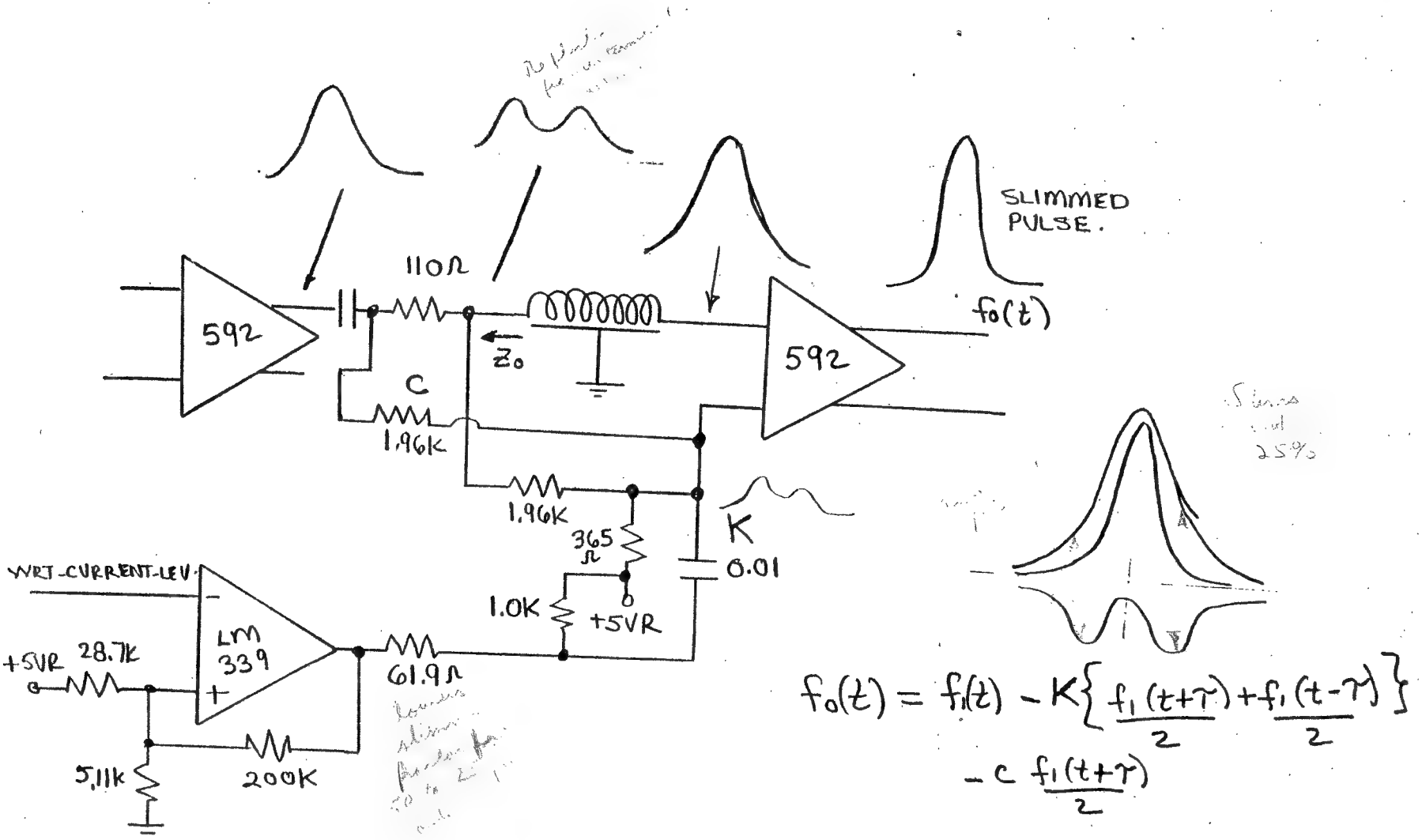
WRITE DATA SIGNAL PATH

- VARIABLE WRITE CURRENT AS A FUNCTION OF CYLINDER ADDRESS.
  - OPTIMIZES WRITE PROCESS.
  - CURRENT CHANGES EVERY 8 CYLINDERS.
  - MICROPROCESSOR CONTROLLED.
  - INNER RADIUS (CYL 656) - 50 M.A. PEAK-TO-PEAK.
  - OUTER RADIUS (CYL 0) - 65 M.A. PEAK-TO-PEAK.
- UNSAFE CIRCUITRY
  - GUARANTEES DATA INTEGRITY.
  - PREVENTS ACCIDENTAL DATA DESTRUCTION.



WREN PREAMP. BLOCK DIAGRAM

MILANES, LT 82



$$f_o(t) = f_i(t) - K\left\{\frac{f_i(t+\tau)}{2} + \frac{f_i(t-\tau)}{2}\right\} - C\,\frac{f_i(t+\tau)}{2}$$

WREN PULSE SLIMMER

MILANES, E J 1982

HD 2^2 J3-06	HD 2^1 J3-04	HD 2^0 J3-32	MEDIA SELECTED		SSI 115
0	0	0	TOP HEAD	BOTTOM MEDIA	22,23
0	0	1	BOTTOM HEAD	MIDDLE MEDIA	20,21
0	1	0	TOP HEAD	MIDDLE MEDIA	18,19
0	1	1	BOTTOM HEAD	TOP MEDIA	16,17
1	0	0	TOP HEAD	TOP MEDIA	14,15

NOTE - A "1" CORRESPONDS TO 0 TO 0.4 VOLTS IN THE INTERFACE.

DURING READ AN INVALID HEAD SELECT INPUT CODES (5,6 AND 7) HAVF THE EFFECT OF NO SELECTING ANY HEADS. AN UNSAFE IS PRODUCED DURING A WRITE.

WREN HEAD-SELECT ENCODING

WREN READ ANALOG DATA PATH FEATURES

13 — 600 mv Range

- AUTOMATIC GAIN CONTROL IN THE READ PATH FOR EXTENDED DYNAMIC RANGE TO COVER FOR LARGE INPUT SIGNAL VARIATIONS.

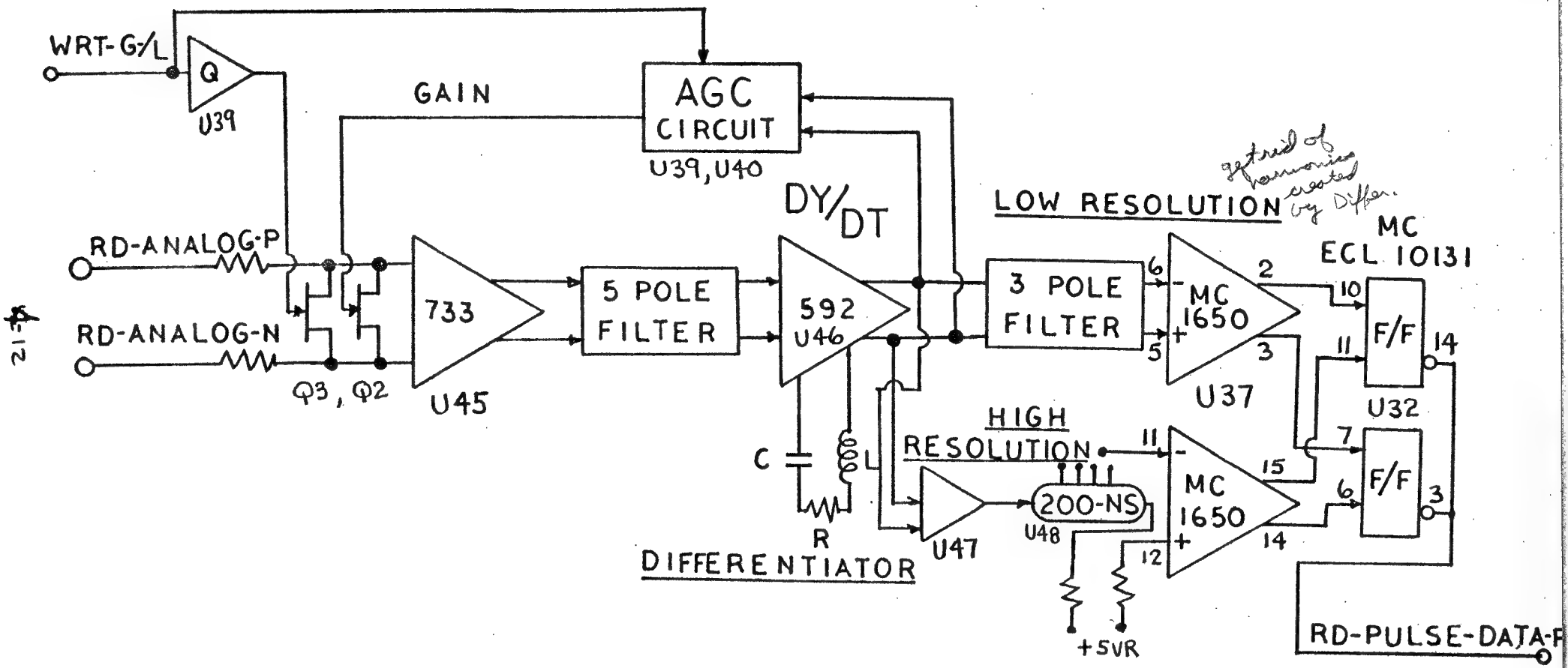
- ACTIVE DIFFERENTIATOR WITH HIGH COMMON MODE REJECTION BY THE USE OF THE 592 VIDEO AMPLIFIER.

- FIVE POLE LINEAR PHASE LOW PASS FILTER FOR HIGH FREQUENCY NOISE REJECTION.

- LOW RESOLUTION PATH WITH A THREE POLE LINEAR PHASE FILTER. THIS FILTER PROVIDES NEEDED MARGIN TO RECOVER SIGNALS FROM VERY HIGH RESOLUTION HEADS AND MEDIA DISTORTIONS TO THE SIGNAL.

- A NEW SINGLE 200 NSEC DELAY LINE IN THE HIGH RESOLUTION PATH WITH 10 NANOSECONDS RESOLUTION.

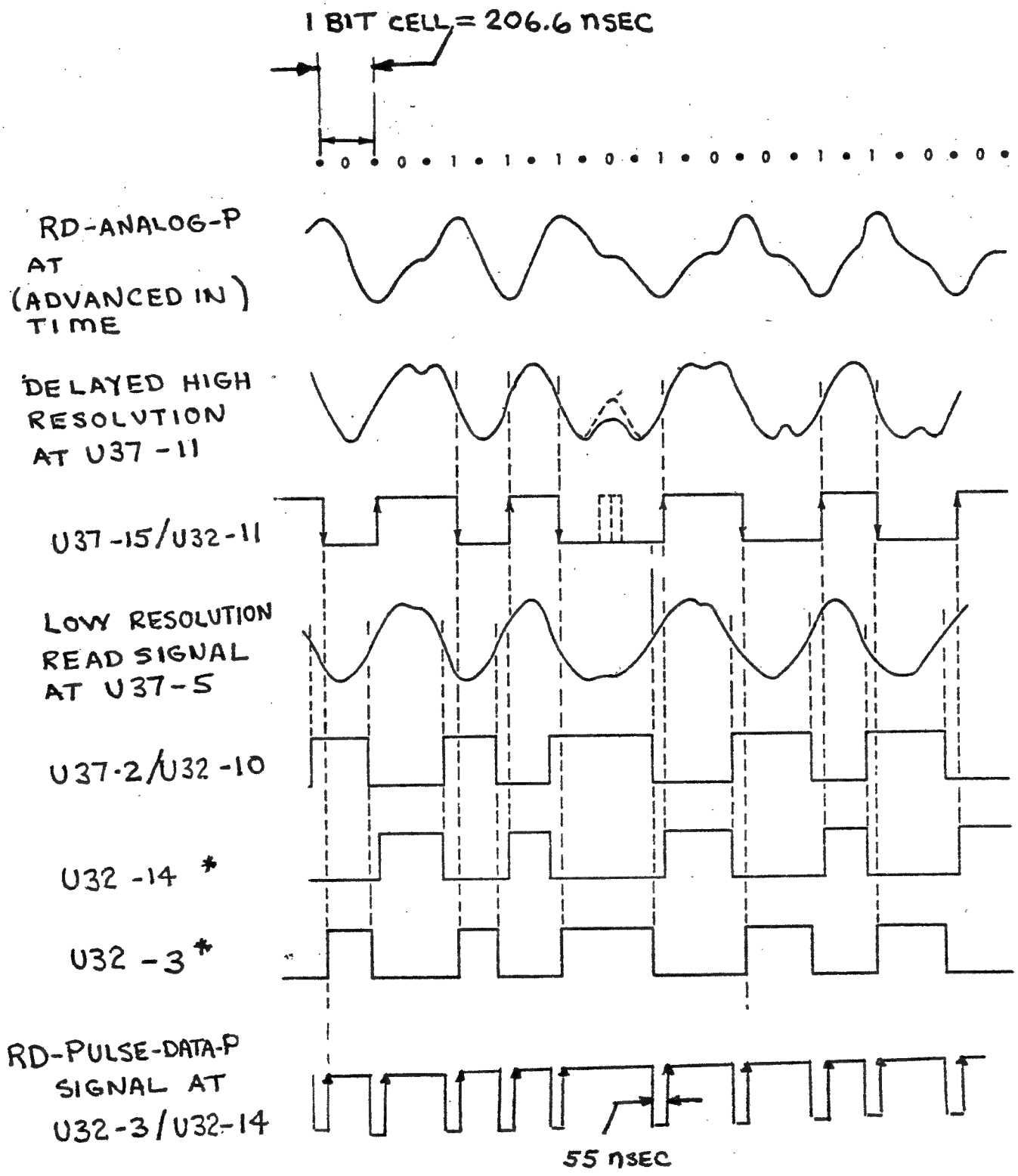
- A DUAL ECL COMPARATOR FOR ACCURATE ZERO CROSSING TIMING AND NO NOISE INJECTION INTO THE ANALOG PATH.



WREN DATA PWA

READ ANALOG

EDDY MILANES 1982



* IF THEY WERE NOT TIED TOGETHER

WREN READ ANALOG WAVEFORM

WREN-3 READ PLO

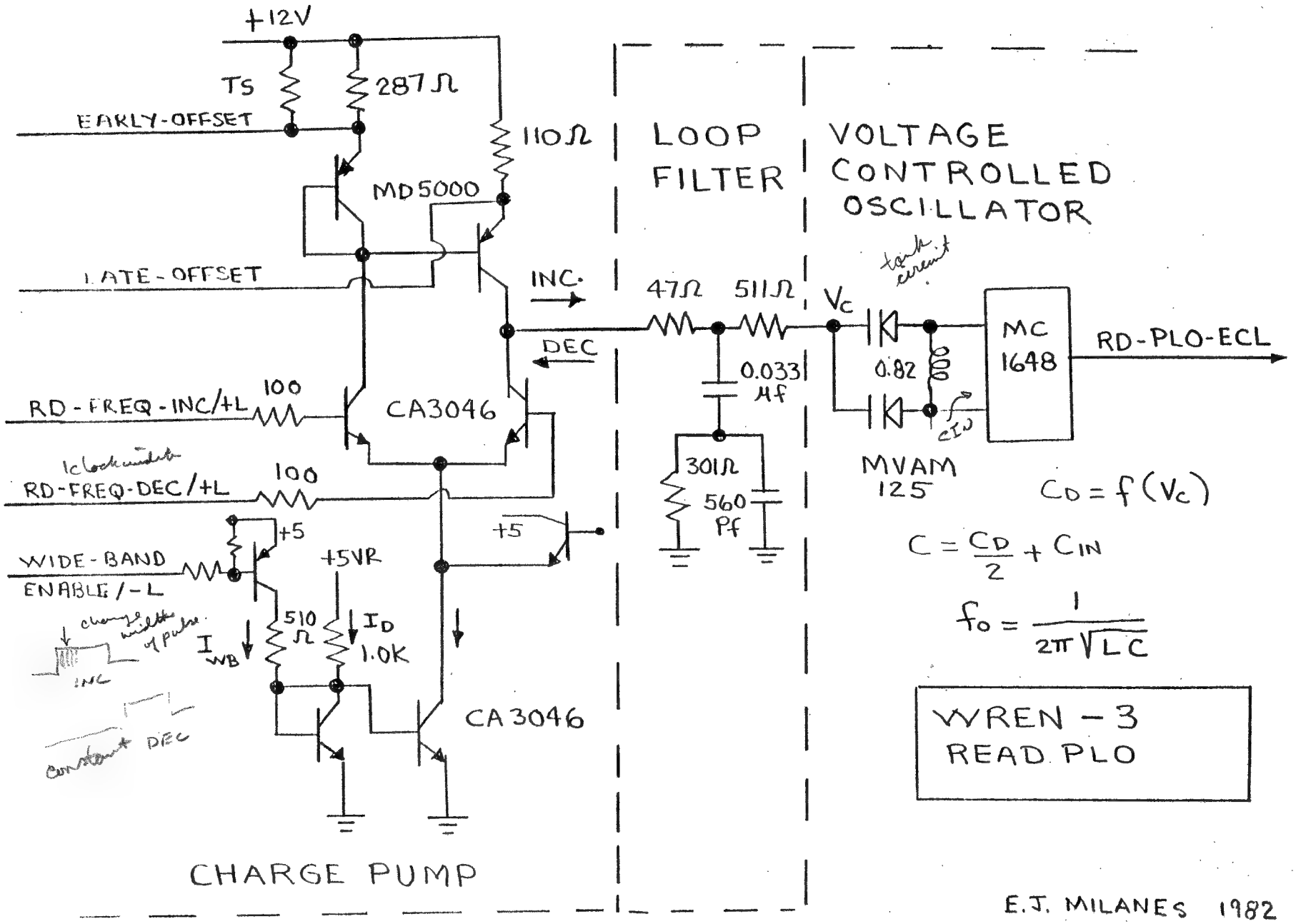
- ON BOARD PLO FOR IMPROVED DATA SEPARATION.

- READ PLO
  - IN CONSTANT FREQUENCY LOCK WITH SERVO PLO THUS LOCKED WITH ACTUAL DISK SPEED.
  - READ PLO FREQUENCY - 19,352 MHZ.
  - SERVO PLO FREQUENCY - 9,676 MHZ.

- PLO CHARGE PUMP
  - USES MATCHED HIGH FREQUENCY TRANSISTORS
    PNP - MD5000
    NPN - CA3046
  - BALANCED BY TEST SELECT RESISTOR DURING PWA TEST TO COMPENSATE FOR PART TOLERANCES.
  - CHARGE PUMP GAIN INCREASED BY WIDE-BAND-ENABLE CONTROL SIGNAL FOR QUICK PHASE LOCK-UP.

- VOLTAGE CONTROLLED OSCILLATOR
  - USES ECL L.C. OSCILLATOR I.C. (MC1648) FOR HIGH SIDEBAND REJECTION
  - INDUCTOR AND VARIABLE VOLTAGE CAPACITORS REDUCE SENSITIVITY TO NOISE USUALLY ASSOCIATED WITH RC OSCILLATORS.

- LOOP FILTER
  - COMPONENTS SELECTED FOR PROPER TRANSIENT RESPONSE AND LOOP BANDWIDTH.


+12V
TS
287Ω
EARLY-OFFSET
110Ω
MD5000
LATE-OFFSET
INC.
DEC
RD-FREQ-INC/+L
100
CA3046
RD-FREQ-DEC/+L
100
+5
WIDE-BAND
ENABLE/-L
+5VR
510Ω
I_{WB}
I_D
1.0K
CA3046
+5
CHARGE PUMP
LOOP FILTER
47Ω
511Ω
0.033 μf
301Ω
560 Pf
VOLTAGE CONTROLLED OSCILLATOR
V_C
MVAM 125
0.82
MC 1648
RD-PLO-ECL
$C_D = f(V_C)$
$C = \frac{C_D}{2} + C_{IN}$
$f_o = \frac{1}{2\pi\sqrt{LC}}$
VVREN-3
READ PLO
E.J. MILANES 1982

WREN READ/WRITE LSI CIRCUIT

FEATURES:

1. CONTAINS THE FOLLOWING LOGIC:
   - WRITE DATA SYNCHRONIZATION LOGIC
   - NRZ/MFM ENCODER
   - WRITE PRECOMPENSATION LOGIC
   - WRITE FAULT DETECTOR
   - READ DATA PHASE/FREQ. DETECTORS
   - WIDEBAND DECODER
   - MFM/NRZ DECODER
   - INTERFACE CLOCK CONTROL

2. MINIMIZES PCB SPACE
   - AVAILABLE IN 40-PIN DIP

3. AVAILABLE IN TWO VERSIONS
   - I^2L AND LSTTL TECHNOLOGIES
   - TWO SEPARATE PART NUMBERS

4. OFFERS LOW POWER DISSIPATION
   - I^2L - 0.85 W
   - LSTTL - 0.90 W

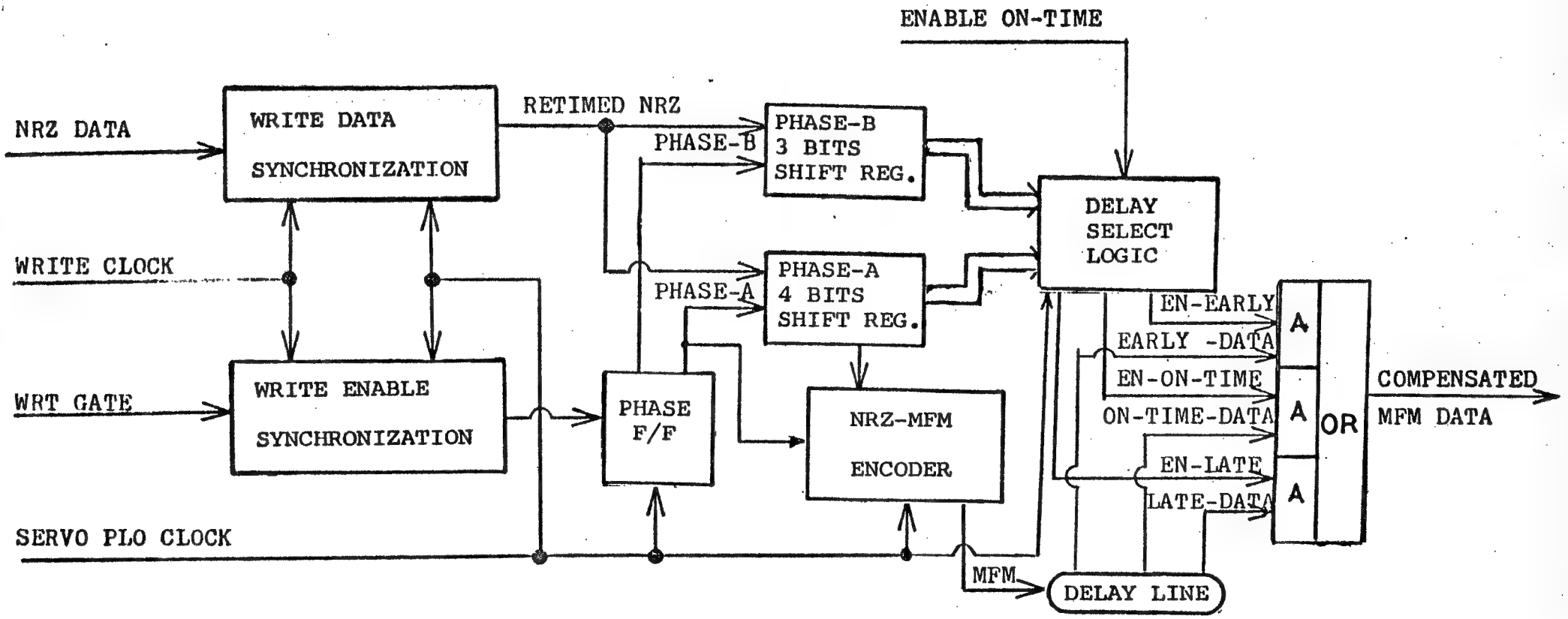
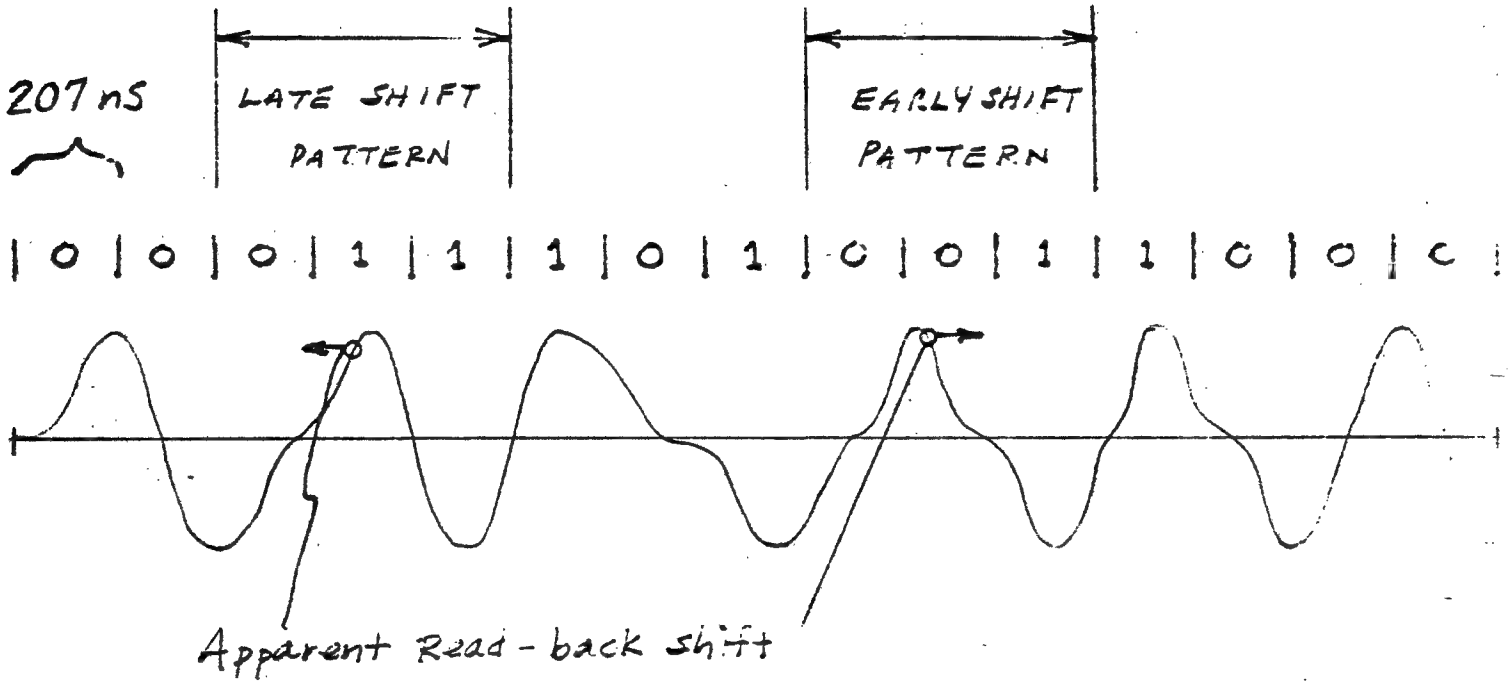


FIGURE 1. MFM ENCODER-COMPENSATOR



WRITE COMPENSATION PATTERNS

LATE SHIFT – 011, 1000

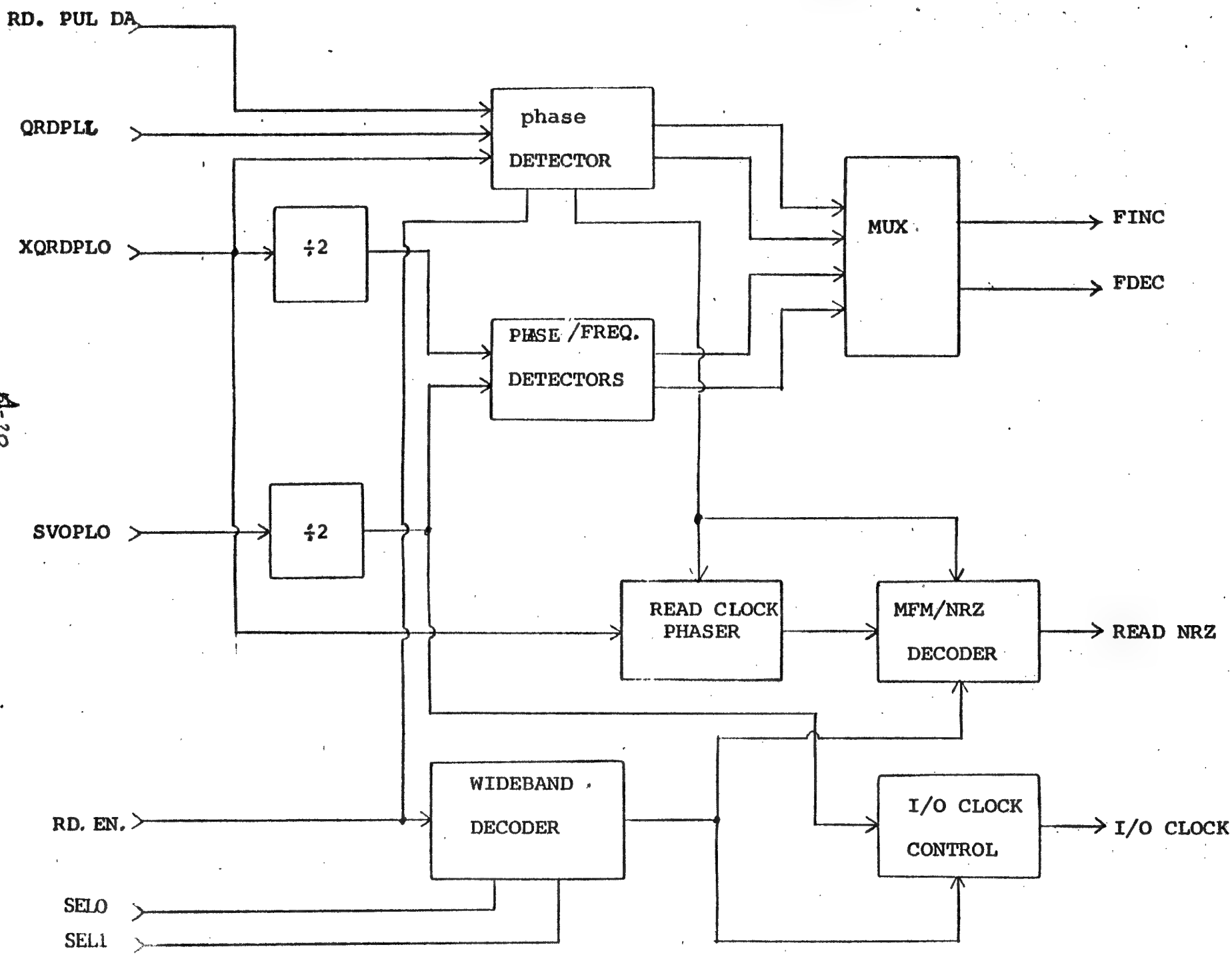
EARLY SHIFT – 10, 001

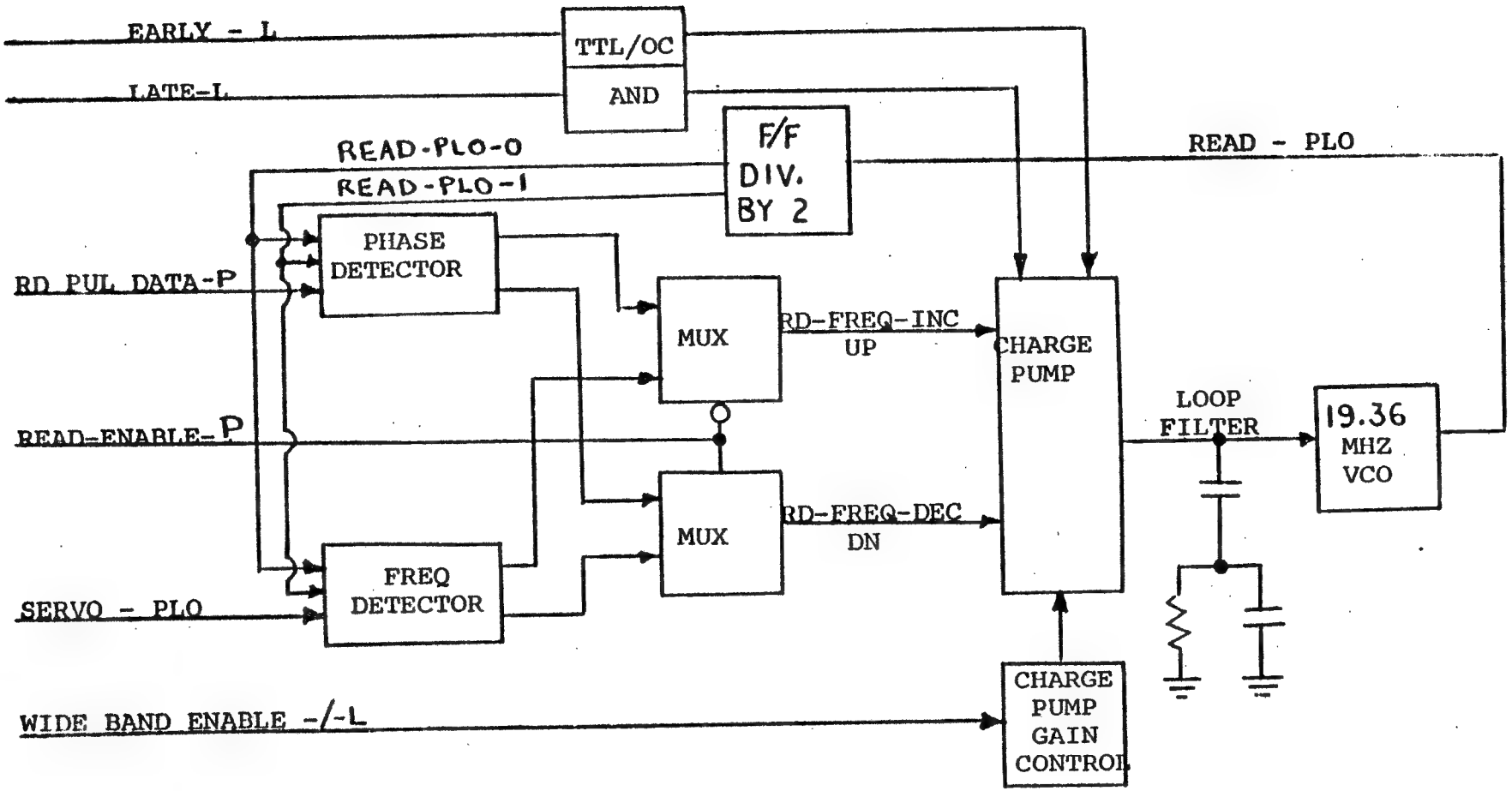
WRITE FAULT DETECTOR

A WRITE FAULT WILL BE GENERATED IF ANY OF THE FOLLOWING CONDITIONS ARE TRUE DURING WRITE ENABLE:

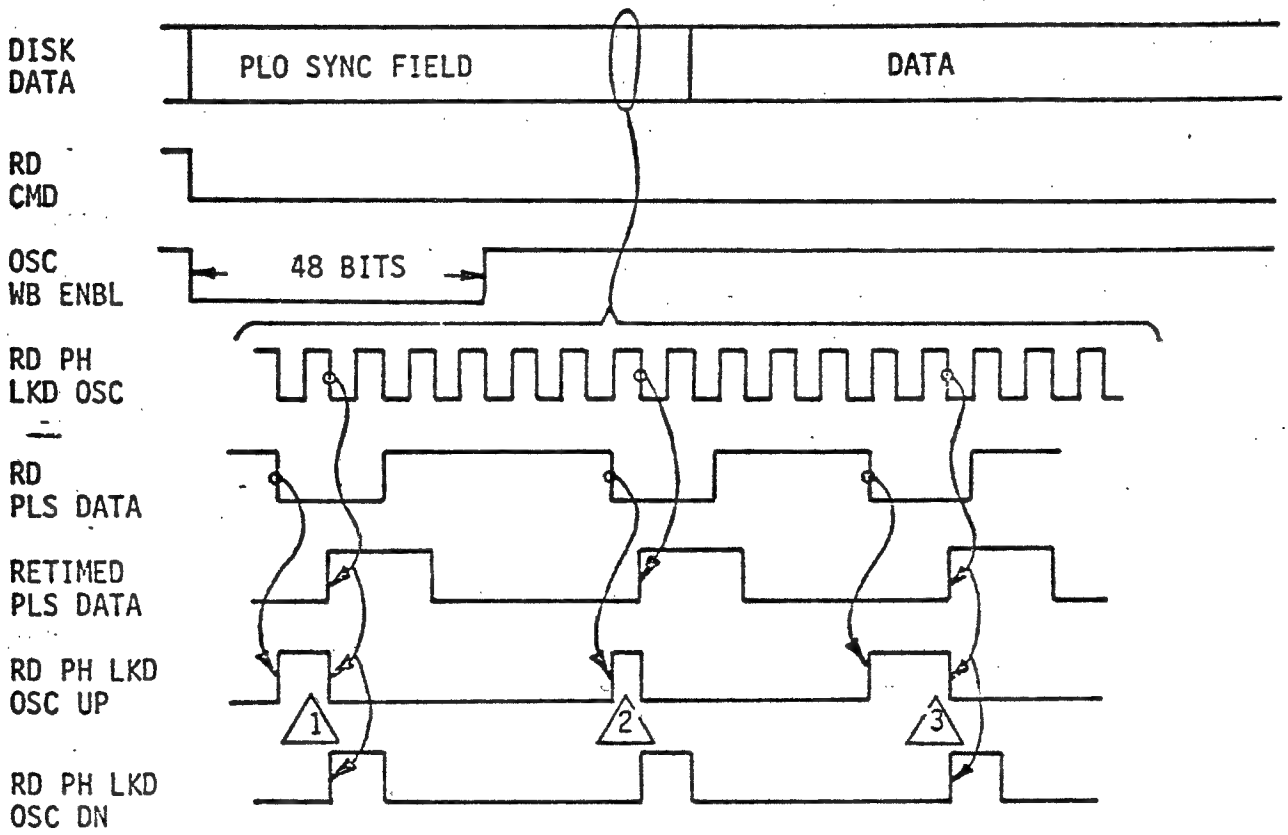
- DRIVE NOT READY
- INVALID HEAD SELECTED
- READ ENABLE ACTIVE
- HEAD UNSAFE PRESENT

READ/WRITE LSI - READ CHANNEL





READ PLO - READ/WRITE OPERATION

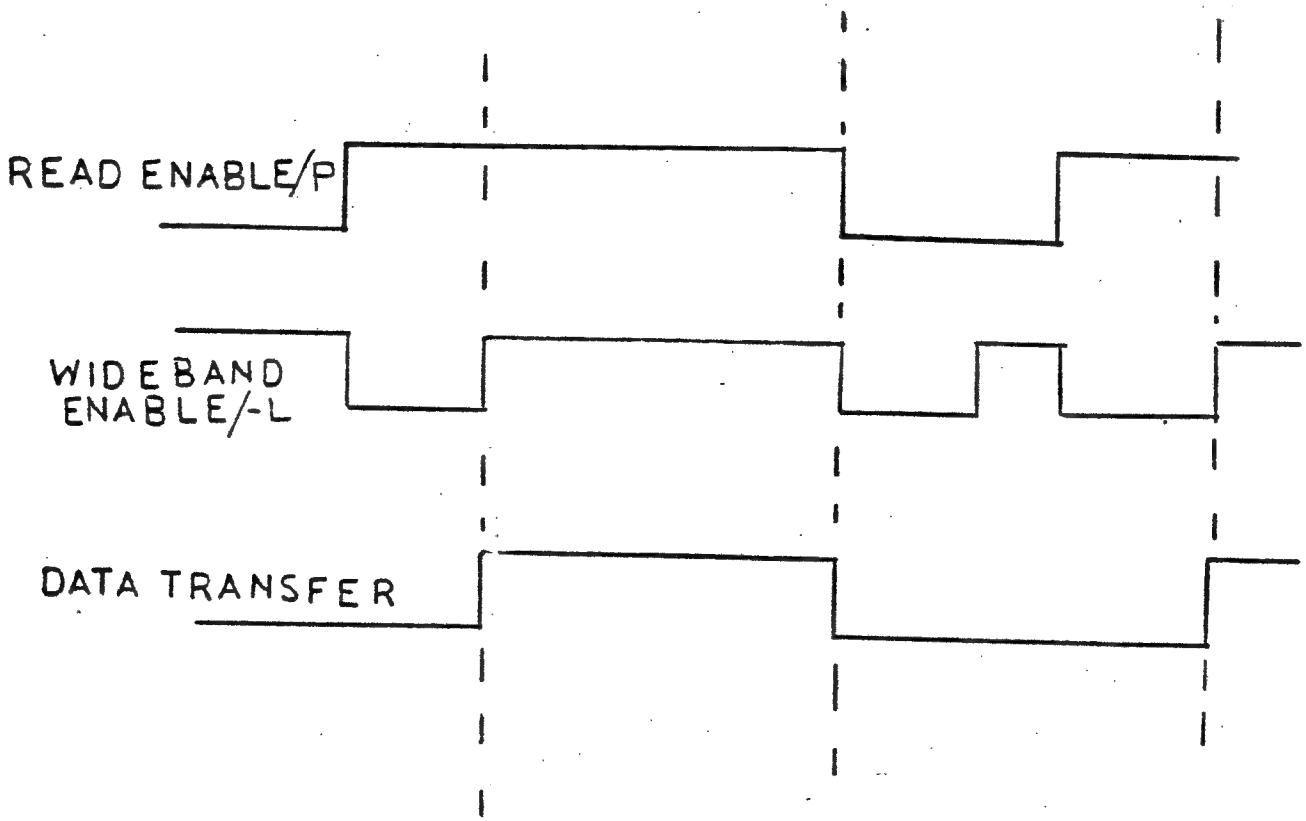


1 PHASE PROPERLY

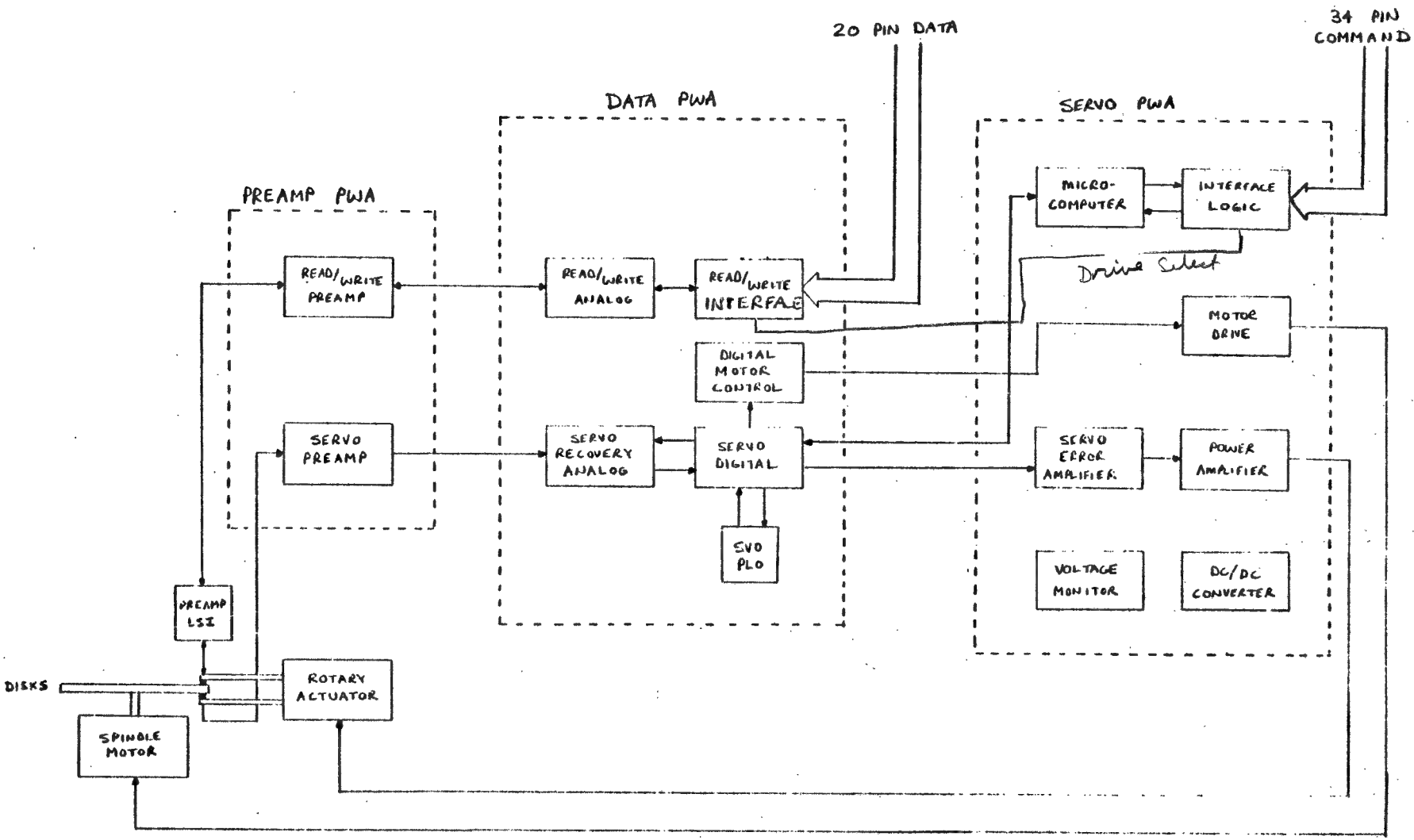
2 READ PLO FAST

3 READ PLO SLOW

PHASE DETECTOR TIMING



WIDEBAND OPERATION



WREN - 5

GENERAL BLOCK DIAGRAM

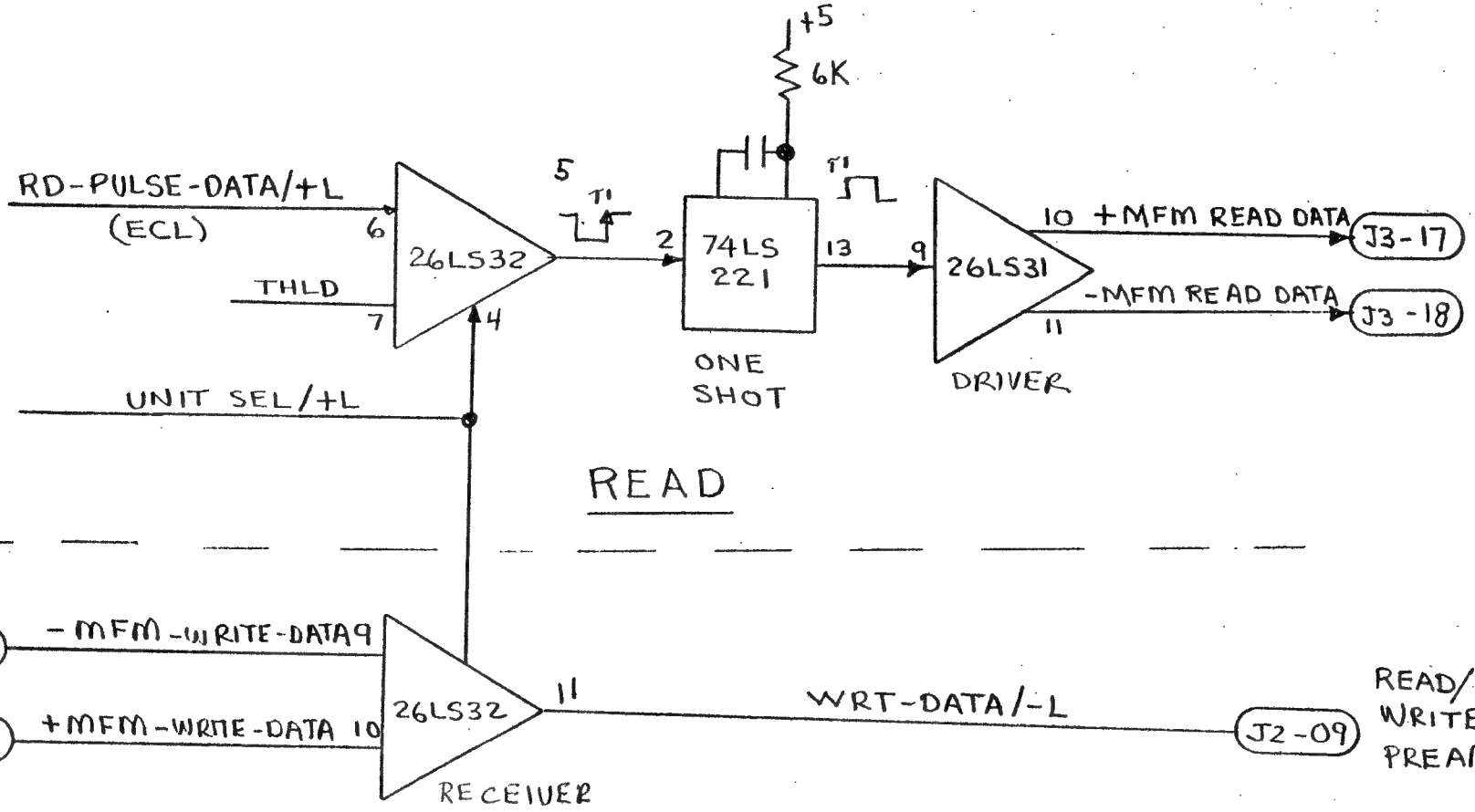
READ/WRITE INTERFACE

CUSTOMER SIGNALS TO DRIVE

- + MFM WRITE DATA
- - MFM WRITE DATA

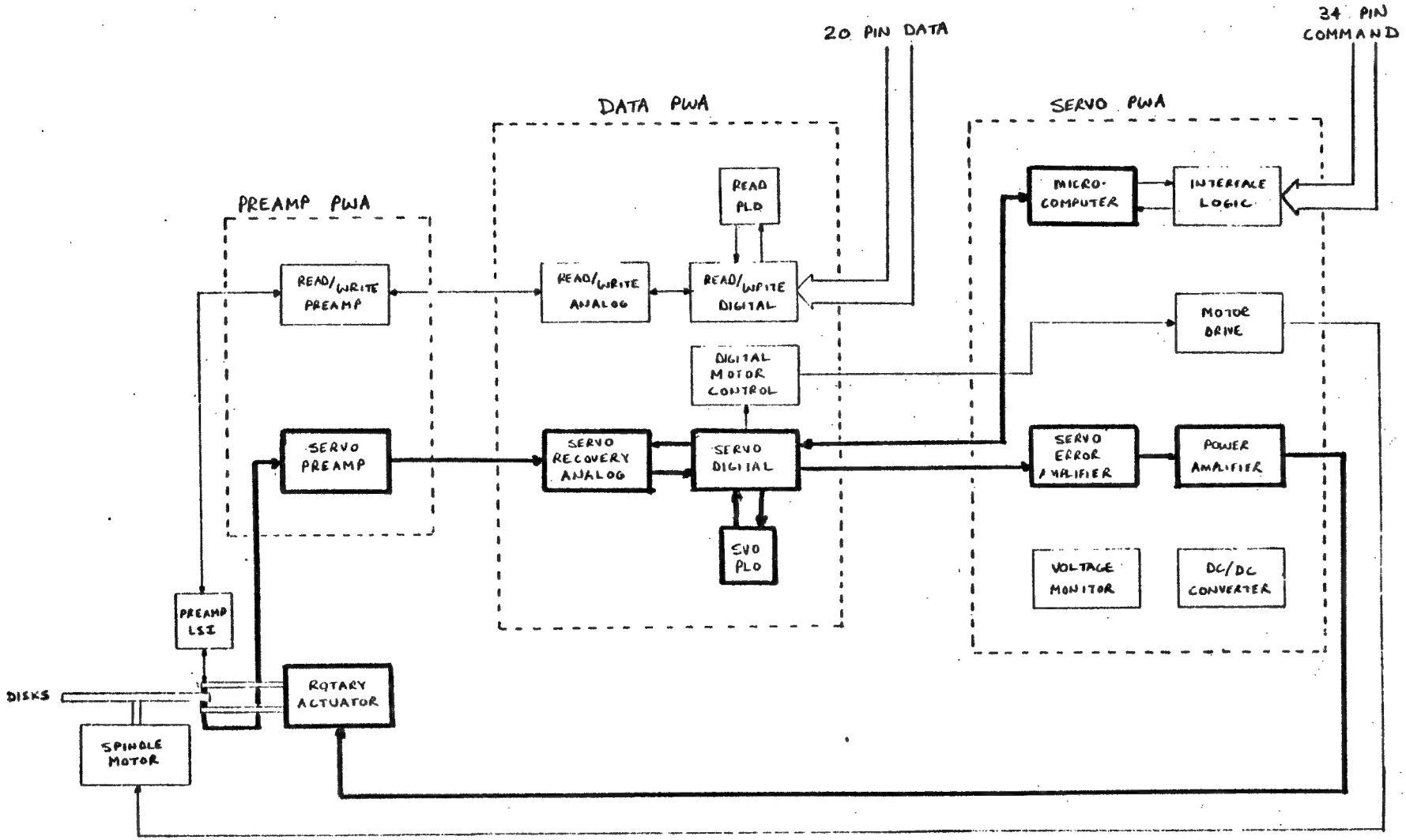
DRIVE SIGNALS TO CUSTOMER

- + MFM READ DATA
- - MFM READ DATA
- DRIVE SELECTED



WREN-5
INTERFACE CONNECTIONS

WREN - SERVO

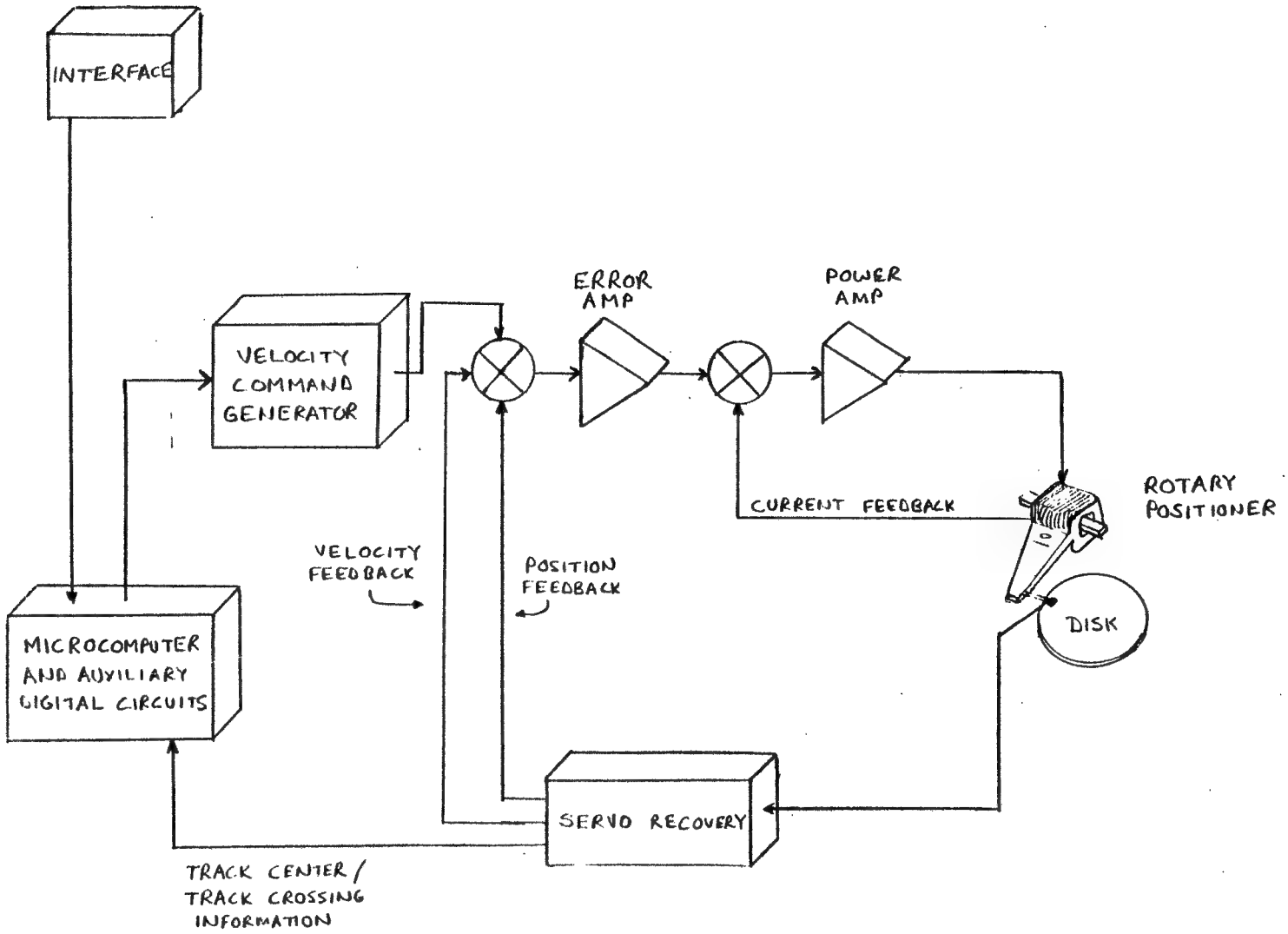


WREN -3

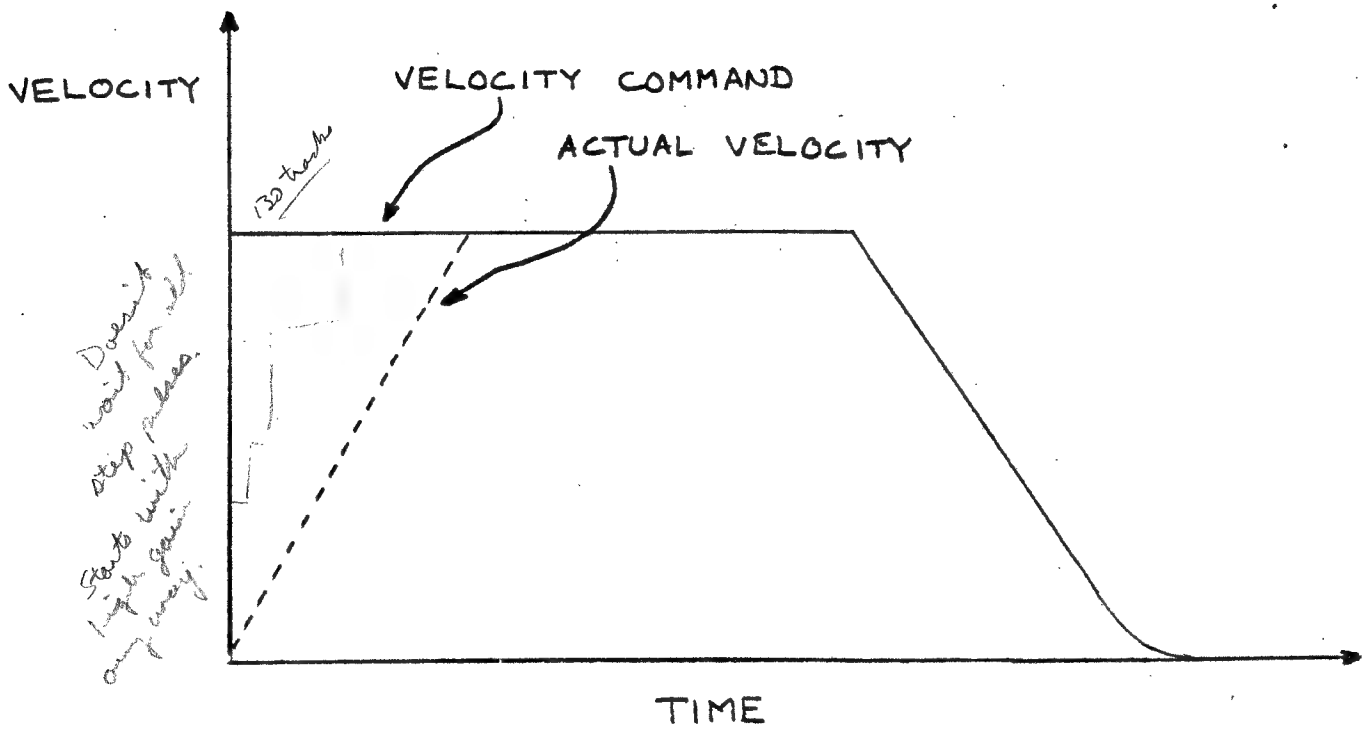
GENERAL BLOCK DIAGRAM

SERVO SYSTEM

- BLOCK DIAGRAM
- FUNCTIONAL DESCRIPTION
  - POSITION LOOP
    - OFFSET MODE
  - VELOCITY LOOP
    - VELOCITY PROFILE
    - AUTO VELOCITY ADJUST
- MICROCOMPUTER
  - I/O DIAGRAM
  - TYPICAL SEEK OPERATION
  - SERVO SURFACE FORMAT
  - POWER ON/HEAD LOAD SEQUENCE
- SERVO ANALOG RECOVERY
  - SERVO DIBIT PATTERN
  - SERVO ANALOG LSI
  - VELOCITY AND POSITION FEEDBACK
- SERVO PLO
- SERVO DIGITAL LSI
- POWER AMPLIFIER
  - SUMMING AMPLIFIER
  - NOTCH FILTER
  - POWER AMPLIFIER
  - SERVO DISABLE/ARM BIAS

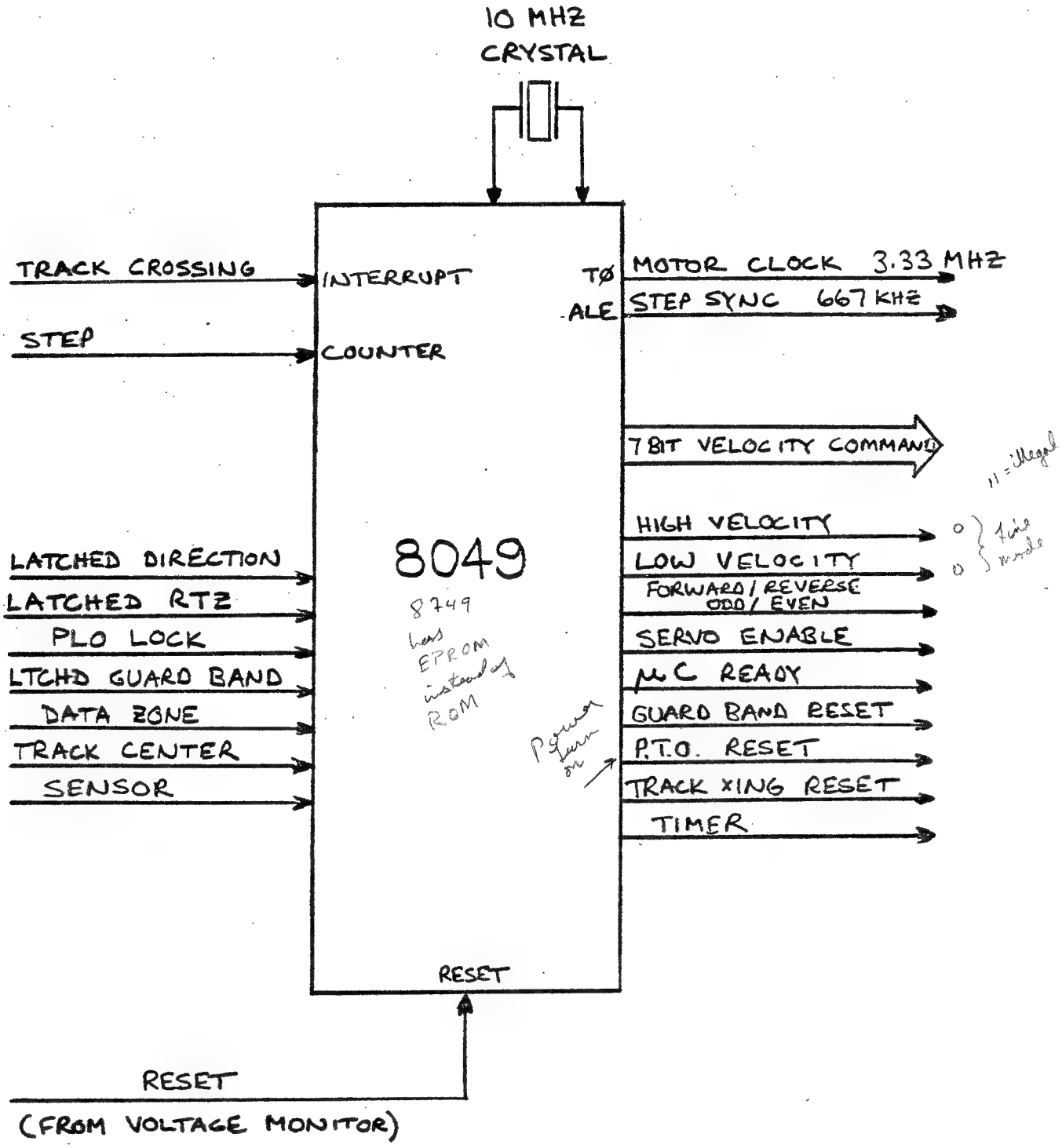


WREN SERVO SYSTEM



TYPICAL VELOCITY PROFILE

from table in computer

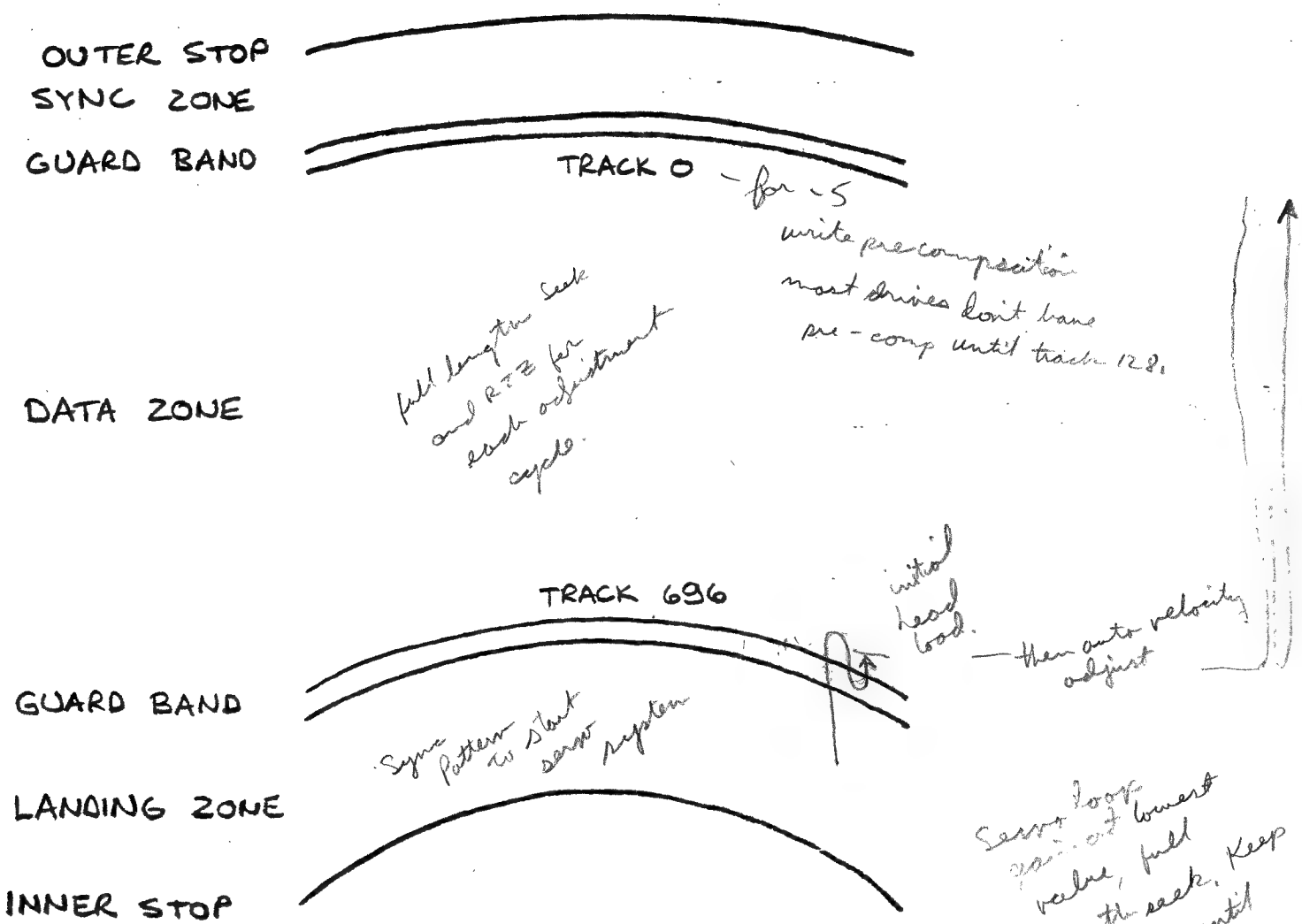


WREN MICROCOMPUTER INTERFACE

12-3-91

TYPICAL SEEK OPERATION

1. MICROCOMPUTER STARTS RECEIVING STEP PULSES.
2. UC GOES NOT READY.
3. UC SAMPLES DIRECTION LINE.
4. UC CALCULATES VELOCITY PROFILE.
5. UC ISSUES VELOCITY COMMAND TO D/A CONVERTER.
6. UC SEES TRACK CROSSING PULSE.
7. REPEAT STEPS 4-7 UNTIL LAST TRACK CROSSING DETECTED. (every track crossing)
8. UC SWITCHES TO FINE (POSITION) MODE.
9. UC WAITS FOR STABLE TRACK CENTER INDICATION.
10. UC GOES READY.

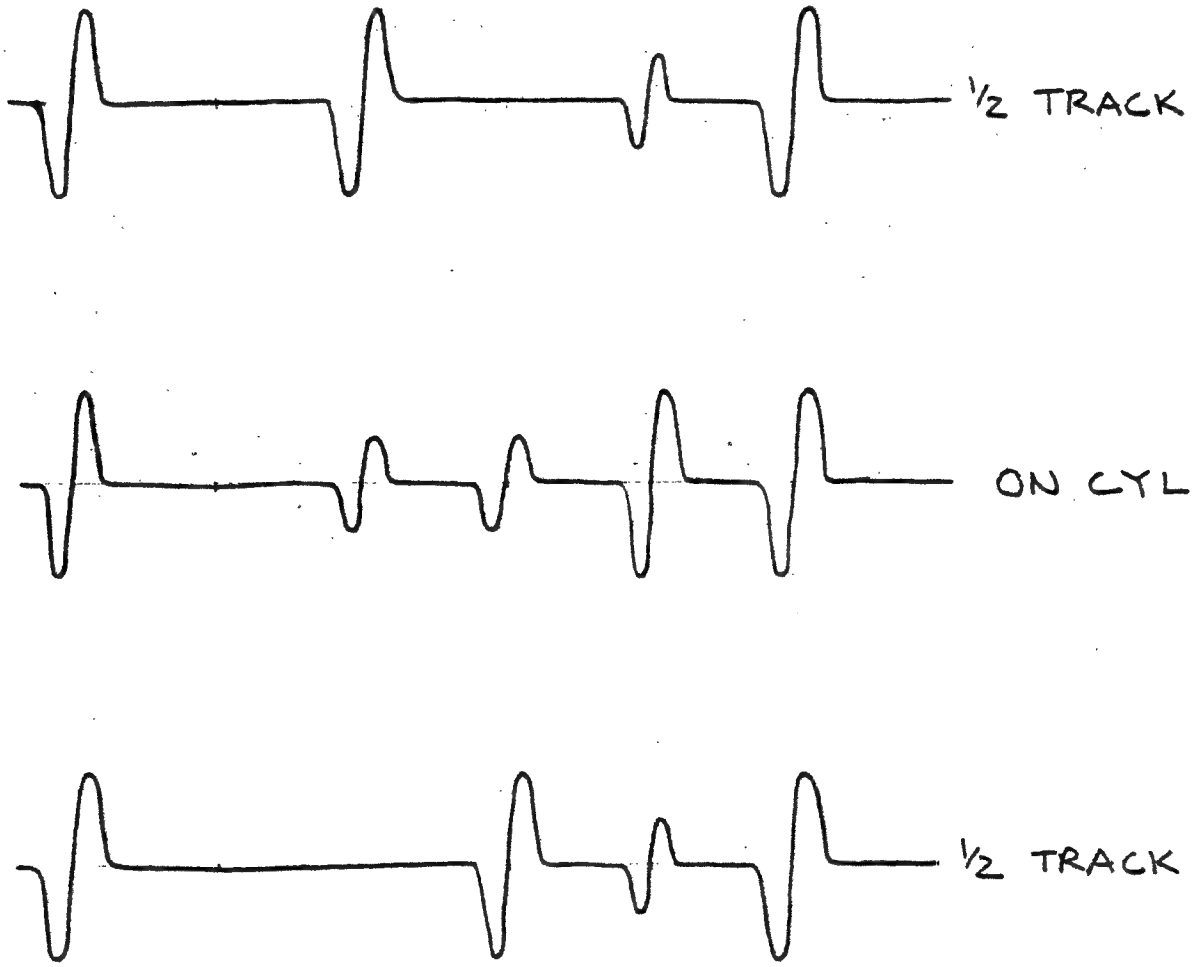


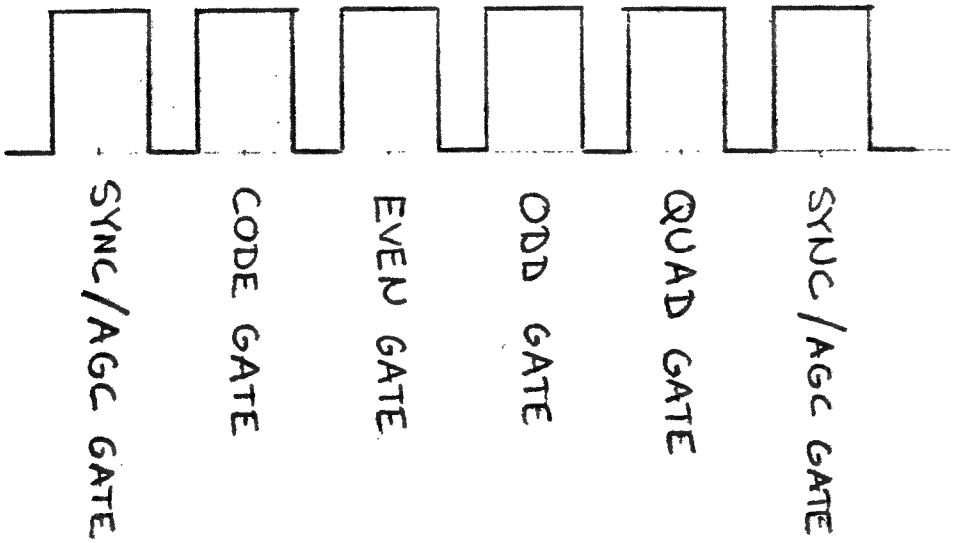
WREN

SERVO SURFACE FORMAT

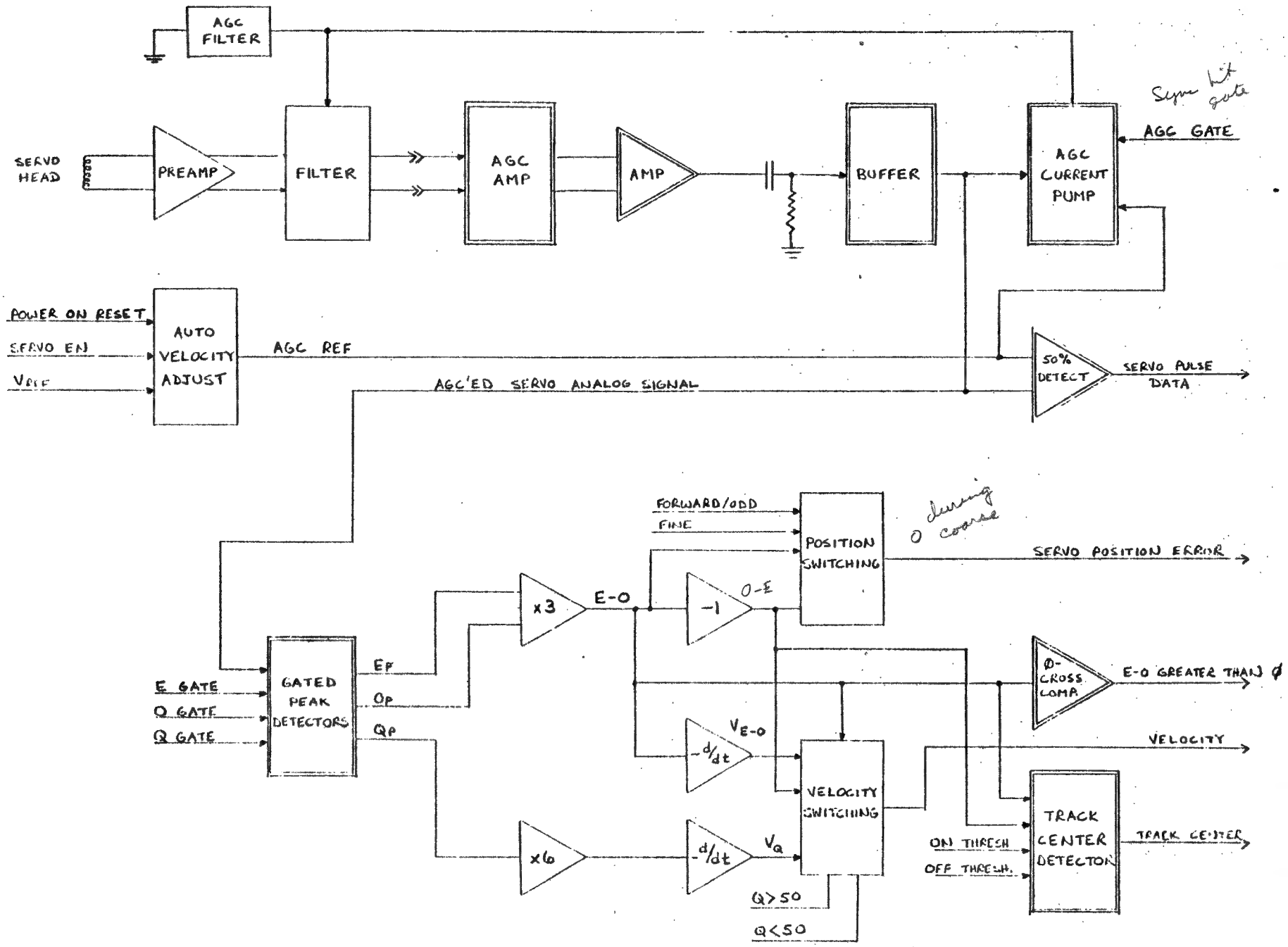
15 nominal
30 max

S C E O Q S

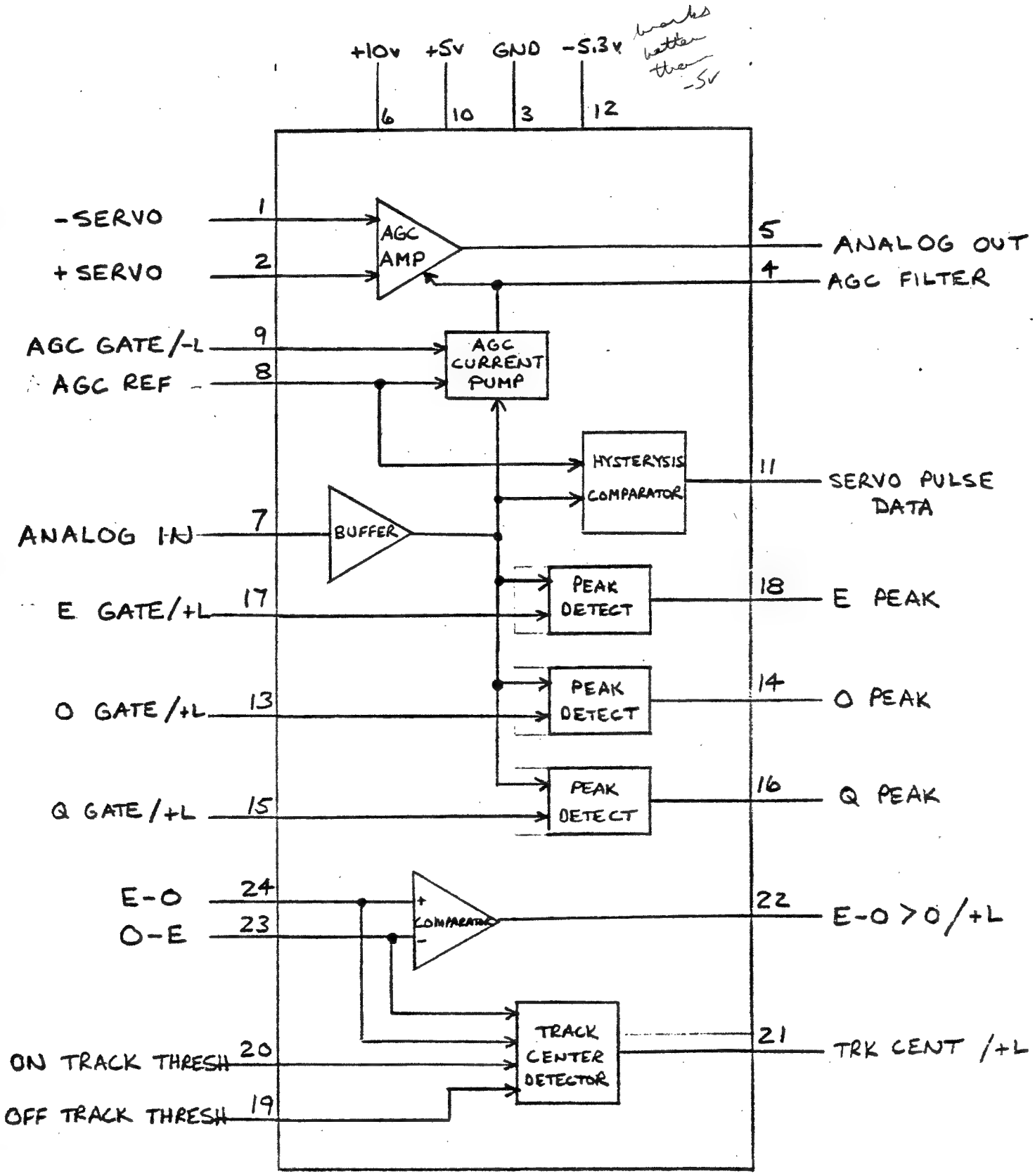




WREN SERVO DIBIT PATTERN



WREN SERVO ANALOG RECOVERY



WREN SERVO ANALOG LSI

WREN SERVO RECOVERY LSI CIRCUIT

FEATURES:

≈ 1000 NAND GATE I^2L

CMOS ≈ 720 CMOS NAND GATES

1. CONTAINS THE FOLLOWING LOGIC:
   - INTERFACE CLOCK GENERATION
   - SERVO DATA GATE DECODERS
   - SERVO PLL PHASE/FREQ. DETECTORS
   - SERVO PLL LOCK DETECTOR
   - INDEX AND GUARD BAND DETECTORS
   - MICROPROCESSOR INTERFACE LOGIC
   - MOTOR CONTROL LOGIC

2. MINIMIZES PCB SPACE
   - AVAILABLE IN 40 - PIN DIP

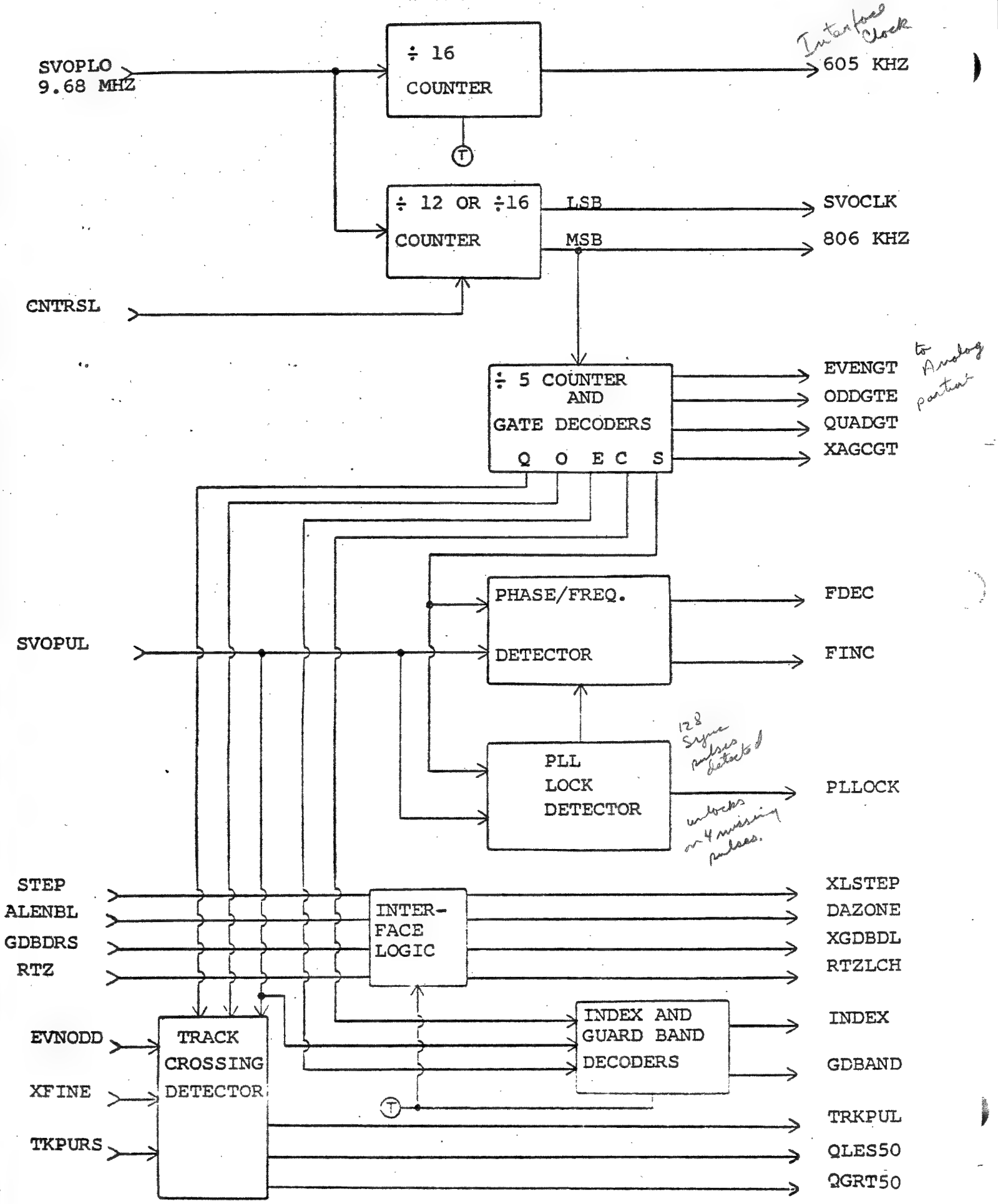
3. AVAILABLE IN TWO VERSIONS
   - I^2L AND CMOS TECHNOLOGIES
   - TWO SEPARATE PART NUMBERS

) INTERCHANGEABLE

4. OFFERS LOW POWER DISSIPATION
   - I^2L - 1.25 W
   - CMOS - 18mW

   ½ to 1/3 cost of I^2L
   ALSO FASTER & CLEANER

WREN SERVO RECOVERY LSI
- EXCLUDING MOTOR CONTROL-



SERVO DATA DECODES

'1' SIGNIFIES SYNC BIT

'0' SIGNIFIES A MISSING SYNC BIT

INDEX DECODE: '111001'

- 1 BIT OF 6 CORRECTABLE

GUARD BAND DECODE: '101010'

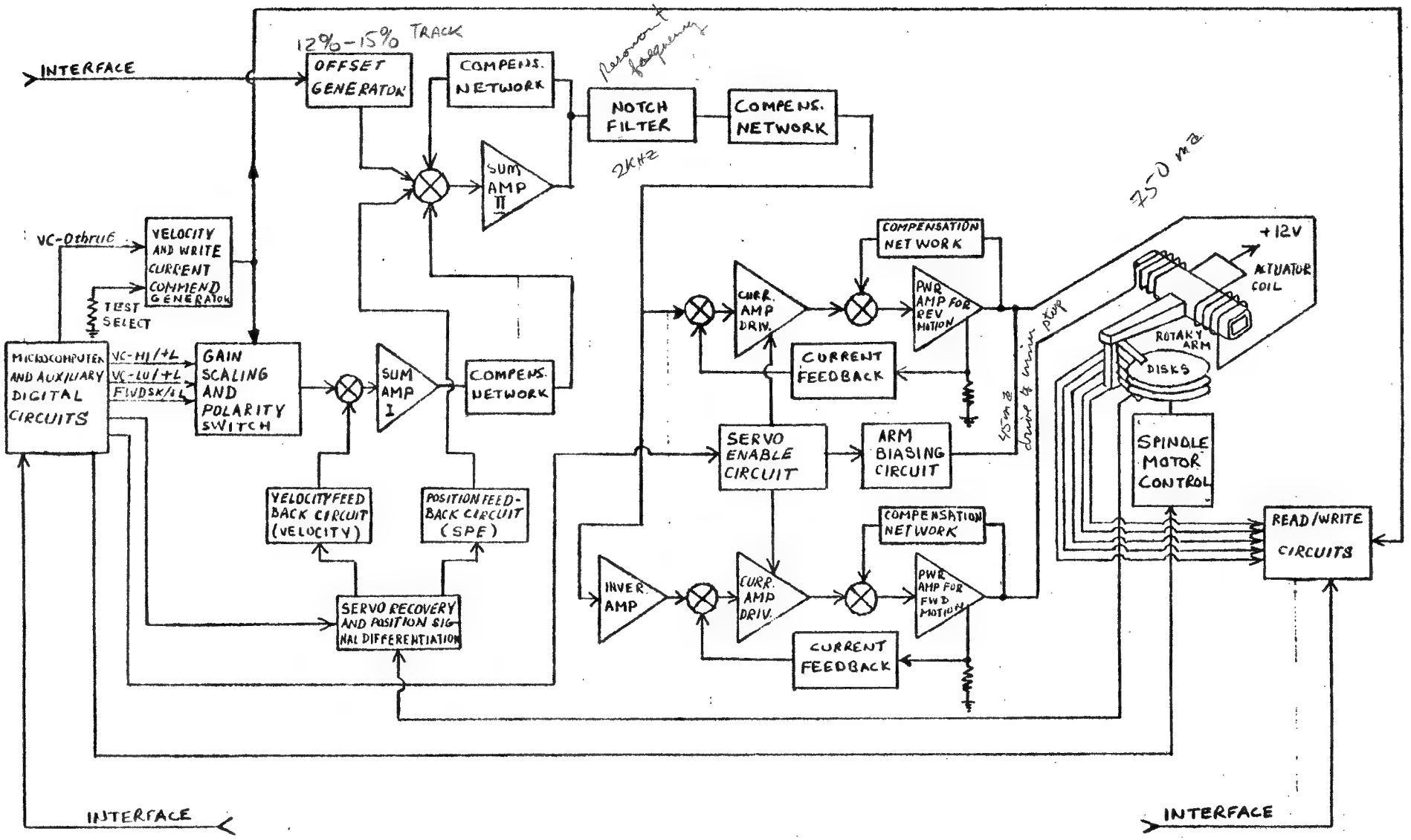
GUARD BAND DROP: '000000'

SERVO PLL LOCK DECODE: '111...1' (X128)

SERVO PLL LOCK DROP: '0000'

MICROPROCESSOR INTERFACE LOGIC

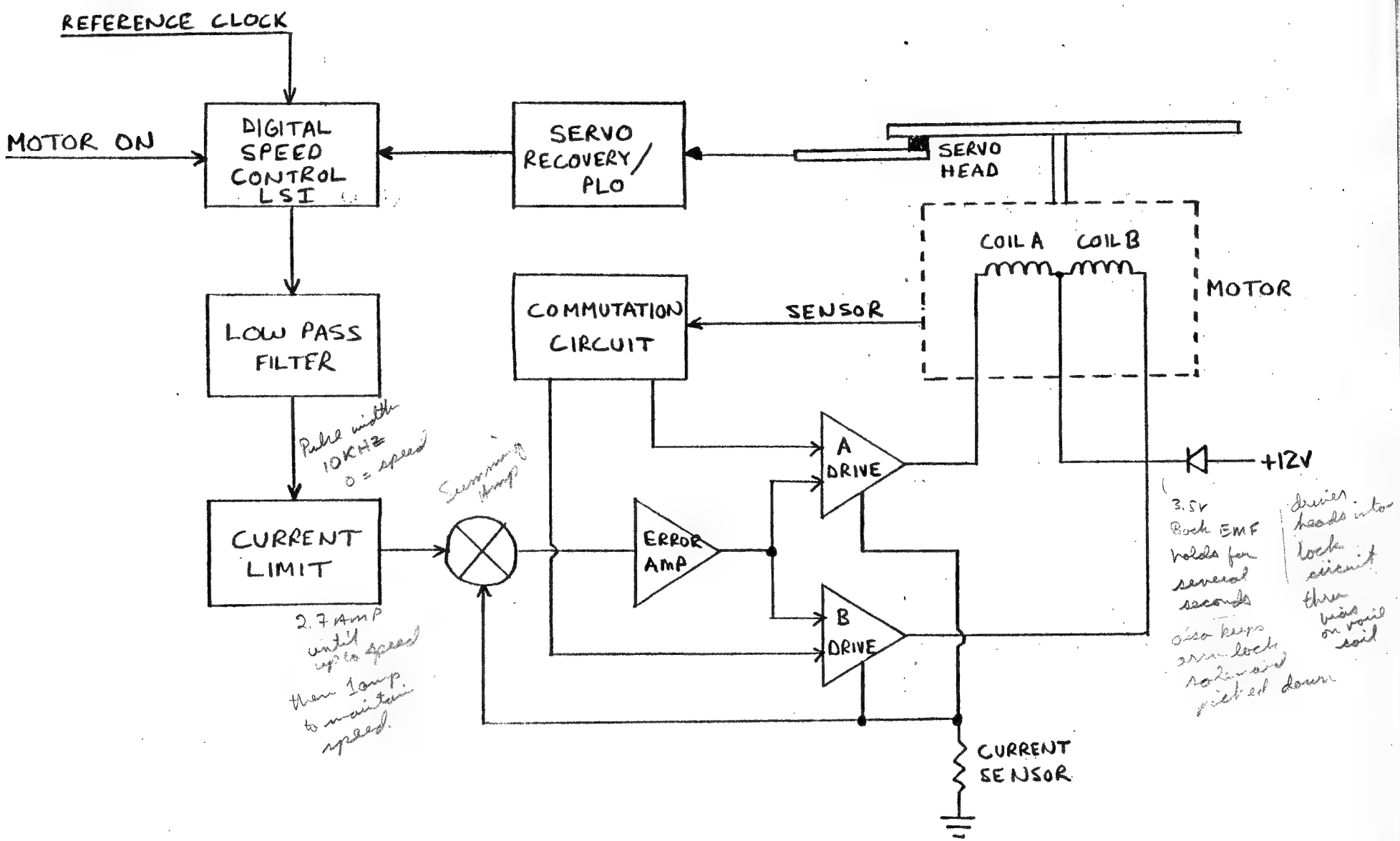
- STEP LATCH - SYNCHRONIZES INCOMING STEP PULSES WITH μP A.L.E. CLOCK.
- DATA ZONE LATCH - SET BY INDEX, RESET BY GAURD BAND.
- GAURD BAND LATCH - SET BY GAURD BAND, μP RESETS.
- RTZ LATCH - SET BY μP, RESET BY GAURD BAND



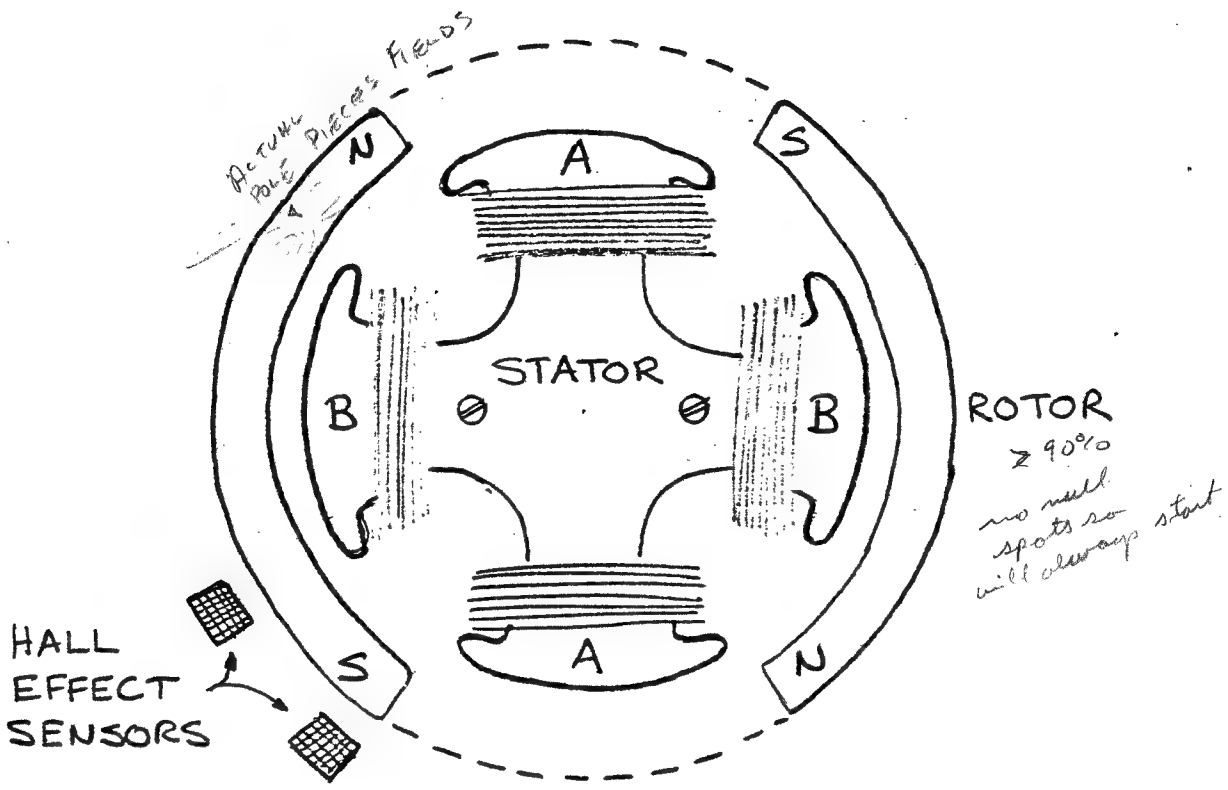
WREN SERVO SYSTEM BLOCK DIAGRAM

SPINDLE MOTOR AND CONTROL

- BLOCK DIAGRAM
- PRINCIPLES OF OPERATION
  - TWO PHASE MOTOR
- DIGITAL SPEED CONTROL IN LSI
- MOTOR DRIVE CIRCUIT
  - CONSTANT CURRENT
  - CURRENT LIMITING
  - LOCKED ROTOR PROTECTION



LIREN SPINDLE MOTOR CONTROL



WREN SPINDLE MOTOR

WREN MOTOR CONTROL LOGIC

1. USES DIGITAL APPROACH
   - CRYSTAL CONTROLLED
   - FEEDBACK DERIVED FROM SERVO SIGNAL
   - ALLOWS IMPLEMENTATION IN LSI CIRCUIT

2. INCORPORATED IN SERVO RECOVERY LSI
   - UTILIZES 30% OF AVAILABLE SPACE
   - DECREASES IC COMPONENT COUNT FROM 18 TO 1

3. SPEED REGULATION - BETTER THAN 0.1% OF 3600 RPM

4. OPERATING RANGE - 7.4 VOLTS TO 15+ VOLTS

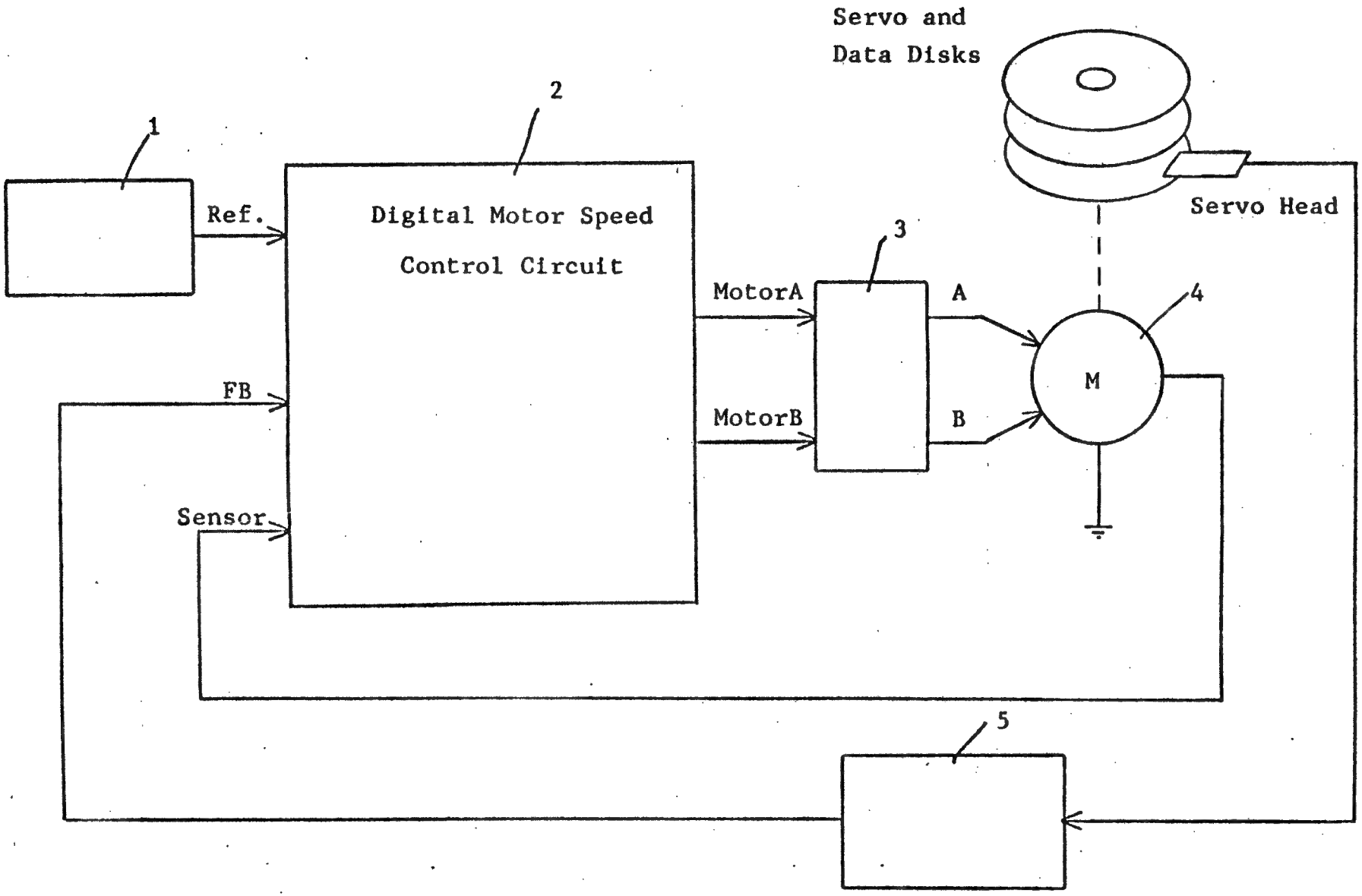


Figure 1: System Block Diagram

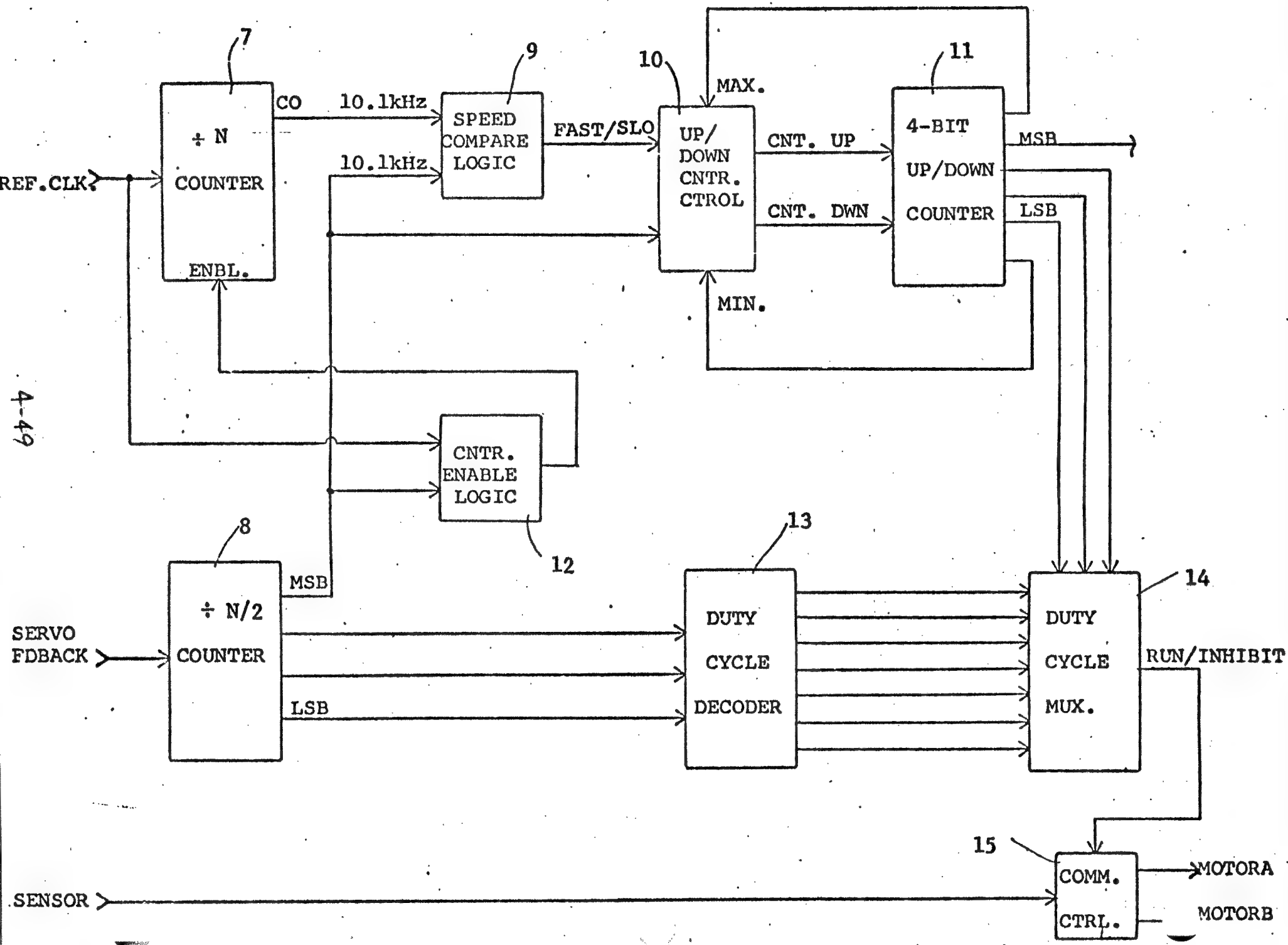

7
÷ N
COUNTER
ENBL.
REF.CLK
CO
10.1kHz
9
SPEED
COMPARE
LOGIC
10.1kHz
FAST/SLO
10
UP/
DOWN
CNTR.
CTROL
MAX.
MIN.
CNT. UP
CNT. DWN
11
4-BIT
UP/DOWN
COUNTER
MSB
LSB
CNTR.
ENABLE
LOGIC
12
8
÷ N/2
COUNTER
MSB
LSB
SERVO
FDBACK
13
DUTY
CYCLE
DECODER
14
DUTY
CYCLE
MUX.
RUN/INHIBIT
15
COMM.
CTRL.
SENSOR
MOTORA
MOTORB

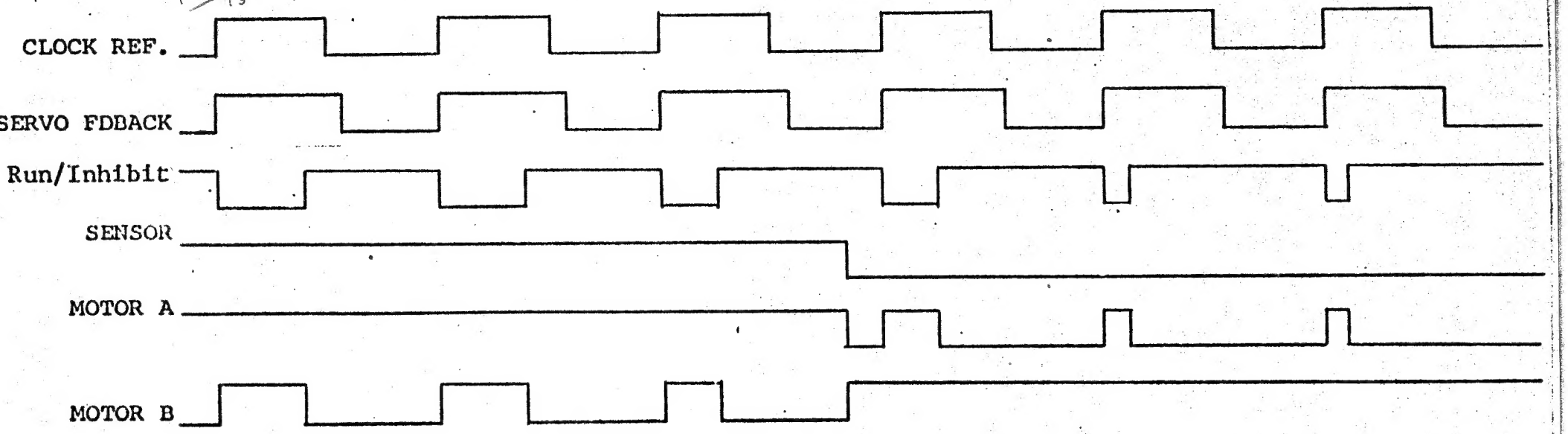
Table 1:

DUTY CYCLE DECODES

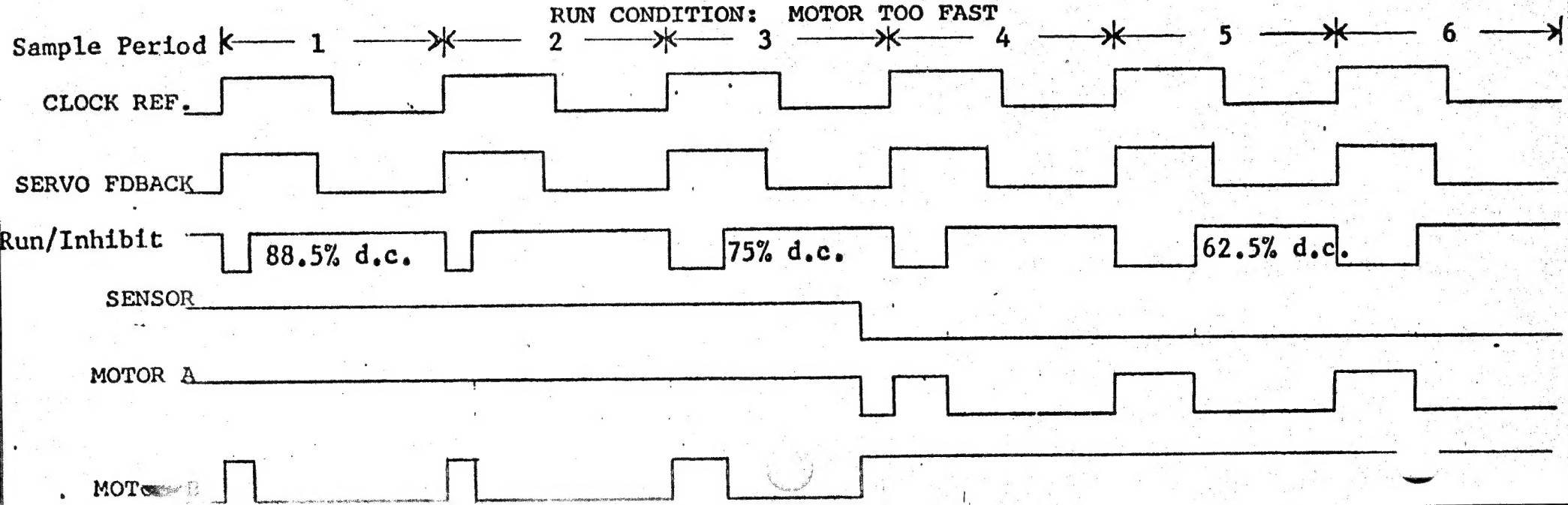
	% OF FULL-ON CONDITION
0	100%
1	88.5
2	75
3	62.5
4	50
5	37.5
6	25

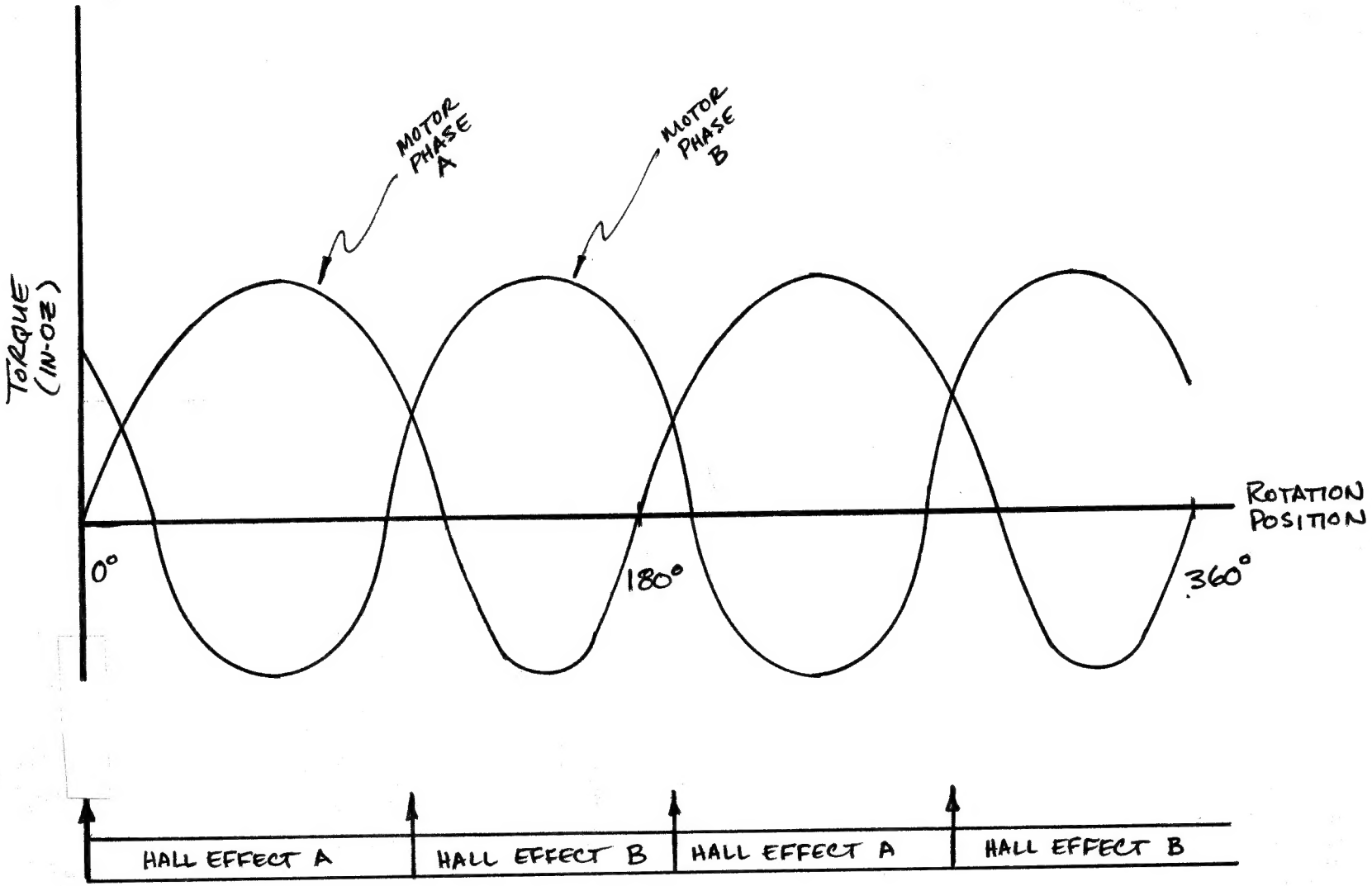
10 MHz
15

RUN CONDITION: MOTOR TOO SLOW



RUN CONDITION: MOTOR TOO FAST





HALL EFFECT SWITCHING

MOTOR START CONCERNS

- UNBALANCED TORQUE

- BRAKE ADJUSTMENTS

CHANGES TO WREN FOR THERMAL CONCERNS

- MOVED ACTUATOR MOUNTING SCREWS CLOSER TOGETHER

  S/N 155

- REPLACED SCREW WITH A PIN

  S/N 262

- POLISHING GIMBLE

- 2.5 MIL GIMBLE

  S/N 155
  REWORKED